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A Design Example of Class-E Based Gate Driver for High Frequency Operation of SiC Power MOSFET

Michihiro Shintani†, Yuchong Sun‡, Hiroo Sekiya‡, and Takashi Sato†

†Graduate School of Informatics, Kyoto University Yoshida-hon-machi, Sakyo, Kyoto 606-8501, Japan
‡Graduate School of Advanced Integration Science, Chiba University Yayoi-cho, Inage-ku, Chiba, 263-8522, Japan
Email: †{shintani,takashi}@i.kyoto-u.ac.jp, ‡aeda4993@chiba-u.jp, sekiya@faculty.chiba-u.jp

Abstract—Design of a class-E based gate driver has been presented for high frequency power converters using SiC power MOSFETs. Through numerical experiments, it is demonstrated that the proposed gate driver can eliminate its switching loss by zero voltage switching (ZVS) operation.

1. Introduction

Silicon Carbide (SiC) is a promising material for realizing high-frequency switching power converters [1]. Increasing the switching frequency allows us to reduce the size of converters. However, as switching frequency increases, switching loss of gate drivers becomes a big issue. Soft switching techniques, such as ZVS operation of class-E amplifiers [2], is one of the effective solutions to minimize the switching loss.

In this paper, we propose a novel gate driver based on class-E amplifier to drive SiC MOSFETs. By achieving the ZVS condition, the proposed gate driver eliminates the switching loss. Based on the equations described in [2], analytical equations for the gate driver application are also proposed to determine component values of the gate driver, such as conductors and inductors.

2. Gate driver design based on Class-E amplifier

Figure 1 shows the topology of the proposed gate driver for driving an SiC power MOSFET. It consists of dc supply voltage $V_{\rm dd}$, dc-feed inductance $L_{\rm f}$, shunt capacitance $C_{\rm S}$, gate resistance $R_{\rm g}$ and an ideal switch. $C_{\rm x}$ is a capacitance to adjust capacitance in the resonance loop and L is the inductance of the resonant circuit. As shown in Fig. 1, the SiC power MOSFET can be regarded as an equivalent circuit with an internal resistor $r_{\rm g}$ and the input capacitance $C_{\rm iss}$ (the sum of the drain-source capacitance $C_{\rm ds}$ and the drain-gate capacitance $C_{\rm gd}$). Thus equivalent capacitance becomes $C_{\rm x}||C_{\rm iss}$. The overall topology of the gate driver circuit is considered as a class-E amplifier. The switch turns on at zero voltage, and thus the energy loss of the gate driver can be reduced.

3. Design constraints

Component values of the proposed gate driver circuit can be determined basically by following the equations of class-E amplifiers. However, two constraints have to be additionally considered for driving the gate electrode of SiC power MOSFETs: (1) achieve resonance under the change of $C_{\rm iss}$ depending on drain-source voltage $V_{\rm ds}$ and gate-source voltage $V_{\rm gs}$, (2) sufficiently large gate current $I_{\rm g}$ to switch the SiC MOSFET.

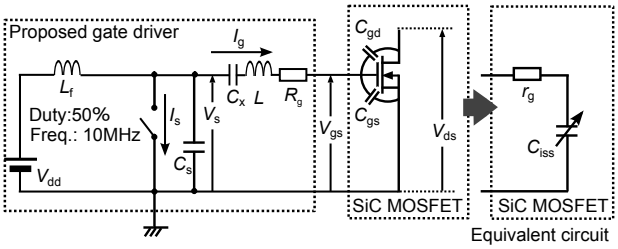

Figure 1: Circuit topology of the proposed gate driver.

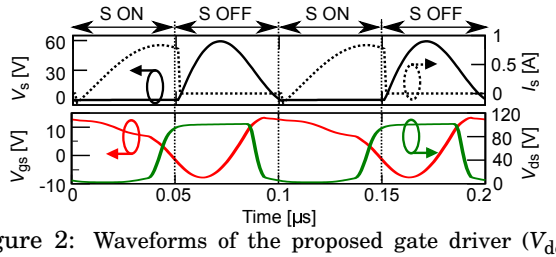

Figure 2: Waveforms of the proposed gate driver ($V_{\rm dd}$ = 17.5 V, $L_{\rm f}$ = 30μH, L = 1.83μH, $C_{\rm s}$ = 149 pF, $R_{\rm g}$ = 18.5Ω, $r_{\rm g}$ = 4.5Ω, α = 0.25, $C_{\rm iss}$ = 552 pF).

By introducing $C_{\rm x}$, these constraints can be simultaneously satisfied. With a small value of $C_{\rm x}$, input capacitance can be made relatively constant. In the proposed design expressions, constant $\alpha(<1)$ is introduced to scale $C_{\rm x}$ as $C_{\rm x} = \alpha \cdot C_{\rm iss}$. Also, to turn on (off) the SiC MOSFET, $C_{\rm iss}$ has to be fully charged (discharged). The required charge amount of $C_{\rm iss}$ can be calculated once accurate $C_{\rm iss}$ model is available, such as those in [3].

4. Numerical experiments

Figure 2 shows simulation waveforms of an example design driving a resistive load of 50 Ω using SiC MOSFET model [3]. The drain voltage is 100 V, and the switching frequency is 10 MHz.

Component values are determined on the basis of the analytical equations. As shown in Fig. 2, there is no overlap between the switch voltage $V_{\rm s}$ and the switch current $I_{\rm s}$. The switching loss of the gate driver can be successfully eliminated by class-E configuration.

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References [1] Baliga, Springer, (2008). [2] Sokal, QEX, (2001). [3] Zhou, et al., NOLTA, (2016).