2016 International Symposium on Nonlinear Theory and Its Applications,
NOLTA2016, Yugawara, Japan, November 27th-30th, 2016

A three-variable ultralow-power analog silicon neuron circuit

Takashi Kohno† and Kazuyuki Aihara†

†Institute of Industrial Science, University of Tokyo
4–6–1 Komaba, Meguro-ku, Tokyo 143-8505, Japan
Email: kohno@sat.t.u-tokyo.ac.jp, aihara@sat.t.u-tokyo.ac.jp

Abstract—A silicon neuronal network is a most fine granular approach to the neuromorphic systems whose significance is growing as a candidate for the core technology of the next generation low-power, autonomous, and intelligent computing systems. In silicon neuron circuits, there has been a trade-off between the power consumption and the capability of reproducing complex neuronal activities. We developed an ultralow-power silicon neuron circuit that can realize multiple classes of neuronal activities including square-wave bursting. Simulation results of our circuit in a square-wave bursting setting are reported.

1. Introduction

The growing social demand for huge-scale information networks and the environmental demand for reducing the power consumption of computing systems are enhancing the significance of neuromorphic systems which realize a low-power, autonomous, and robust computing by mimicking the information processing of the brain. A silicon neuronal network is a most fine granular approach to the neuromorphic systems, which aims to realize an electronic-circuit version of the nervous system by connecting silicon neuron circuits via silicon synapse circuits.

The electrophysiological activity of the neuronal cells is one of the crucial factors in the information processing of the nervous system. Therefore, various models with different levels of details have been developed. The ionic conductance models which describe the mechanisms for the dynamical change of the membrane potential can precisely reproduce complex neuronal activities. Silicon neuron circuits for bio-silico hybrid systems implement them[1, 2] and inherit this advantage. But the complexity in their equations rises their power consumption beyond 100 μW. For low-power consuming systems, simpler models have to be adopted. Many low-power silicon neuron circuits implement the integrate-and-fire(I&F)-based models and consume just several nanowatts[3, 4, 5, 6, 7]. The equations of these models are generally simple because they treat the neuronal spike as an event and describe only its timing. It is shown that networks of the I&F-based silicon neurons can execute various processing similar to those by the artificial neural networks[3, 4, 6].

In the brain, however, the neuronal spikes are not uniform[8, 9] (graded response) and chemical synapses can transmit their variation to their postsynaptic cells[10]. Thus, there is a possibility that the analog information of neuronal spikes is playing some roles in the information processing of the brain. Another class of simple neuronal models that do not ignore the spike generation mechanisms is the qualitative models. They describe the dynamical structures in the neuronal activities by relatively simple polynomial-based equations. In our previous works[11, 12, 13, 14, 15], we proposed to design an implementation-oriented qualitative neuronal model that is described by formulae of the input-output characteristics of low-power circuits. On the basis of this approach, we developed a three-variable qualitative silicon neuron model for implementation by subthreshold metal-oxide-semiconductor field-effect transistor (MOSFET) analog circuits. It supports multiple classes of neuronal activities including the Class I and II in Hodgkin's classification, the regular spiking, the square-wave bursting (SWB), and the elliptic bursting by appropriate configurations of its parameters. A fabricated circuit could realize all of these activities with power consumption less than 72 nW[16, 12, 13, 14, 15]. This power consumption is more than one order of magnitude higher than that of the ultralow-power circuits in [17] (2 nW) which was designed by a similar approach but dedicated only to simplest activities, either Class I or Class II.

Because a wide variety of complex neuronal activities are observed in the brain, it is natural to suppose that the capability of reproducing more complex activities is important for the brain-like computing. Hence, to reduce the power consumption penalty paid for this capability, we designed another three-variable model for ultralow-power circuitry by expanding the two-variable model of the silicon neuron circuit in [11] that supports only the Class I and II. In this article, we report simulation results of its implementation in a SWB setting. The model and circuitry of our circuit are explained in the next section. The simulation results are reported in the third section followed by conclusion.

2. Model and Circuitry

Our silicon neuron model has three variables, v, n, and q. The first two variables are for the spike generation dynamics and the last variable provides slow feedback dynamics that modifies the former faster dynamics. Its equations are

$$C_v \frac{dv}{dt} = f_v(v) - g_v(v) + I_{av} - r_n(n) - r_q(q) + I_{\mathrm{stim}}, \quad (1)$$

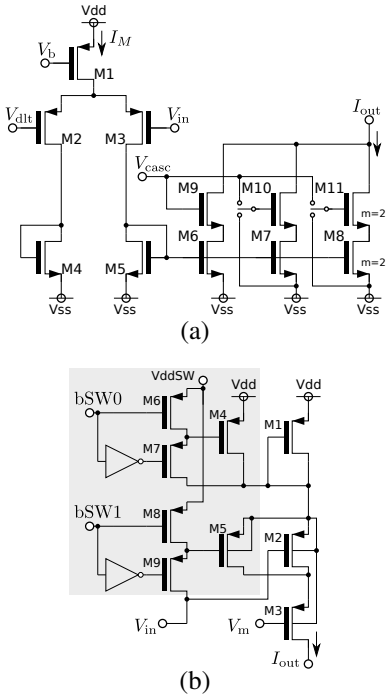

Figure 1: Schematics of (a) $f_x(v)$ circuit and (b) $g_x(v)$ and $r_y(y)$ circuits, where $m = 2$ (1) for M3 in the $g_x(v)$ ($r_y(y)$) circuits. The circuit in the gray box is implemented only for the $g_n(v)$ circuit.

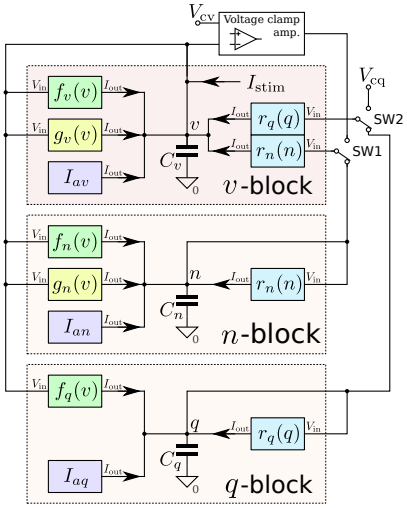

Figure 2: Block diagram of our silicon nerve membrane circuit. Each block corresponds to a term in the system equations (1) and (2).

$$C_n \frac{dn}{dt} = f_n(v) - g_n(v) + I_{an} - r_n(n), \quad (2)$$

$$C_q \frac{dq}{dt} = f_q(v) + I_{aq} - r_q(q), \quad (3)$$

where v, n, and q represent the membrane potential, the fast dynamics, and the slow dynamics, respectively. Capacitances C_v, C_n, and C_q are 0.6 pF, 0.9 pF, and 24 pF, respectively. Currents I_{av}, I_{an}, and I_{aq} are parameters and $I_{\rm stim}$ is a stimulus input. Functions $f_x(v)$, $g_x(v)$ ($x = v, n$), and $r_y(y)$ ($y = n, q$) are the formulae of the input-output characteristics of transconductance circuits whose schematic is illustrated in Fig. 1. Their equations are

$$f_x(v) = \frac{M_x}{1 + \exp\left(-\frac{\kappa}{U_T}(v - \delta_x)\right)}, \quad (4)$$

$$g_x(v) = I_0 \sqrt{\frac{R_{x20} \exp\left(\frac{\kappa}{U_T}\theta_{gx}\right)}{1 + R_{x21} \exp\left(-\frac{\kappa}{U_T}(v - \theta_{gx})\right)}}, \quad (5)$$

$$r_y(y) = I_0 \sqrt{\frac{\exp\left(\frac{\kappa}{U_T}\theta_{ry}\right)}{1 + \exp\left(-\frac{\kappa}{U_T}(y - \theta_{ry})\right)}}, \quad (6)$$

where κ, U_T, and I_0 are the capacitive-coupling ratio, the thermal voltage, and the current scaling parameter of PMOS transistors, respectively. Parameter $\theta_{..}$ depends on voltage $V_{\rm m}$ in Fig. 1(b). Parameters R_{x20} and R_{x21} are controlled by digital inputs bSW0 and bSW1 (see Fig. 1(b)), respectively. When bSW0 (bSW1) is low, the gate voltage of M4 (M5) is shorted to VddSW which equals to or is higher than Vdd. In this situation, M4 (M5) is disabled and thus R_{x20} (R_{x21}) is 2. When voltage bSW0 (bSW1) is high, M4 (M5) is activated and thus R_{x20} (R_{x21}) is 4 (1). These parameters are used to change the v-offset of $g_x(v)$. Because the circuit in the gray box is not implemented for $g_v(v)$, R_{v20} and R_{v21} are fixed to 2. These functions have a monotonic increasing sigmoidal shape and the square root in $g_x(v)$ and $r_y(y)$ makes their gradient shallower than that of $f_x(v)$. The reversed N-shaped v-nullcline, which is common in neuronal spike generation systems, is realized by combination of a shallow sigmoidal curve and a steep one.

Figure 2 illustrates the block diagram of our circuit. Each colored box represents the elemental circuit that corresponds to the function in its label. Constant current sources for I_{ax} are implemented by transconductance amplifiers. Each variable in the model is coded by the voltage difference between Vdd (1.0 V) and the non-grounded terminal of the corresponding capacitor. The white box at the top of the diagram is a feedback amplifier for voltage clamp measurement. It clamps v at a voltage similar to $V_{\rm cv}$ when SW1 and SW2 are switched to the upper terminal and $V_{\rm cq}$ is fixed at 1.0 V to keep the output of the upper $r_q(q)$ circuit zero (the voltage clamp mode). The nullcline of each variable is drawn by plotting the voltage that codes the variable while slowly sweeping $V_{\rm cv}$. A bifurcation diagram of the spike generation system can be drawn when SW1 is switched to the lower terminal and SW2 is switched to the upper terminal (the bifurcation diagram mode). In this setting, the circuit for the v-n system operates normally while the output of the $r_q(q)$ circuit can be controlled by $V_{\rm cq}$. By slowly sweeping $V_{\rm cq}$ and plotting the stable state of the v-n system, we can draw a bifurcation diagram whose bifurcation parameter is q. These two modes guide the parameter voltage tuning process to construct the dynamical structure

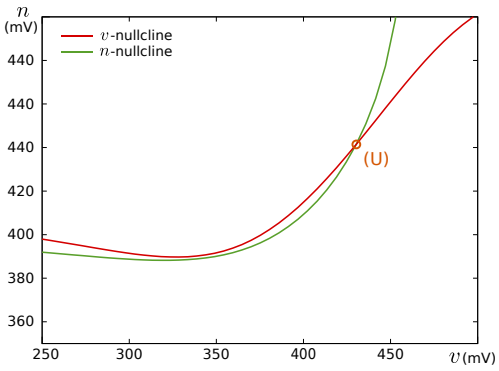

Figure 3: The v- and n-nullclines of our circuit in a square-wave bursting setting, drawn in the voltage clamp mode.

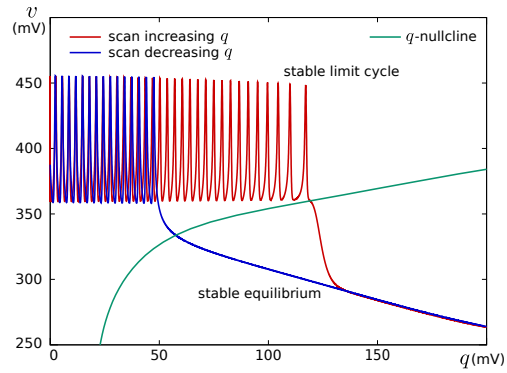

Figure 4: A v-q plane of our circuit. The bifurcation diagram of the v-n system obtained in the bifurcation diagram mode and the q-nullcline measured in the voltage clamp mode are projected.

in a neuronal activity to be realized. They are particularly effective to find appropriate parameter voltages of a fabricated circuit which is affected by the device mismatch.

3. Simulation Results

We designed our silicon neuron circuit using a Taiwan Semiconductor Manufacturing Company (TSMC) 0.25 µm mixed-signal CMOS process development kit and found appropriate parameter voltages for a SWB in the Spectre simulation. Figure 3 shows the v- and n-nullclines drawn in the voltage clamp mode. They are configured to have one intersection when q is 0 and three intersections if the v-nullcline is displaced downward when q is increased. To invoke a saddle-loop bifurcation after this saddle-node bifurcation, the time constant of n is suppressed by keeping V_{m} in the $r_n(n)$ circuit sufficiently high. The stable state of the v-n system is projected on the v-q plane in Fig. 4, which is obtained in the bifurcation diagram mode. The red (blue) curve was obtained by slowly increasing (decreasing) V_{cq}. Bistability between a limit cycle and an equilibrium is seen at the region where q is between 50 mV and 120 mV. The equilibrium point and the limit cycle correspond to the non-spiking and repetitively spiking states, respectively. The sweep time was 2 sec for this diagram. In the increasing sweep, the period of the limit cycle is extended up to infinity as q is increased. Thus, the sweep time has to be extended depending on the required precision in the diagram. The green curve is the q-nullcline obtained in the voltage clamp mode, which is configured to separate these concurrent two stable states. Note that $\frac{dq}{dt}$ is positive (negative) above (below) the q-nullcline. When the state point is attracted by the equilibrium, it slowly moves leftward until the equilibrium vanishes at near q = 50 mV (the silent phase). Then, the state point is attracted by the limit cycle (the spiking phase). It slowly moves rightward until the limit cycle vanishes at near q = 120 mV and attracted by the equilibrium again. This alternation of the silent and spiking phases is the mechanism of the SWB. We observed a regular bursting (Fig. 5(a)) similar to that in the SWB cells[18, 19]. It is known that the tonic firing and the chaotic bursting are observed in the Hindmarsh-Rose model, a qualitative SWB model, when a parameter for the slowest variable is modified[20]. Our circuit could produce these activities (Figs. 5(b) and (c)) by appropriately tuning a parameter voltage that controls M_q. In all these settings, the average power consumption was less than 4.9 nW.

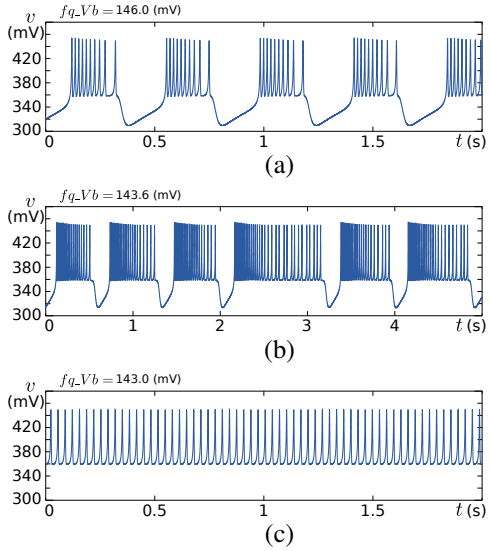

Figure 5: Waveform examples of v in a square-wave bursting setting. (a) Regular bursting (the parameter voltages are the same as those in Figs. 3 and 4). (b) and (c) Chaotic bursting and tonic firing observed when a parameter voltage is modified.

4. Conclusion

We designed a configurable ultralow-power silicon neuron circuit and verified that it can realize SWB using the Spectre simulator. It has 14 parameter voltages which have to be configured appropriately. For the configuration pro-

Table 1: Comparison of analog silicon neurons (*exact value not shown, **graded response)

	this work	[17]	[4]	[7]
model	QM	QM	I&F	I&F
power	< 5 nW	1.7 nW	< 3 nW*	< 7 nW
area (μm^2)	90000	2740	918	2980
process	0.25 µm	0.35 µm	0.18 µm	90 nm
Class I	√	√	√	√
Class II	√	√		partially
GR**	√	√		
SWB	√			√

cedure, the feedback amplifier and switches are integrated in our circuit. They are used to draw the nullclines and the bifurcation diagrams of the *v-n* system, which provide an effective guide to construct proper dynamical structures. Its power consumption was estimated to be lower than 5 nW, which will be reduced in our future circuits by substituting cascode circuits for the transconductance amplifiers used to generate constant currents. The transconductance amplifiers for I_{av}, I_{an}, and I_{aq} consume 1001 pA, 929 pA, and 313 pA to generate 173 pA, 156 pA, and -32 pA, respectively. The power consumption will be reduced to about 3 nW when the sum of the differences between these currents is saved by this substitution. We are working on ultralow-power parameter voltage generator circuits which consume about 100 pW. If they are integrated into our silicon neuron circuit, the total power consumption will be about 4.4 nW. The difference between it and 1.7 nW in [17] will be the cost for the configurability and the capability of realizing complex neuronal activities. Our circuit occupies larger area than recent analog silicon neurons (see Table 1). However, it may be shrinked by using a finer process because the effects of device mismatch are compensated by our parameter tuning procedure.

Acknowledgments

This study was partially supported by JST PRESTO and CREST program, VLSI Design and Education Center(VDEC), The University of Tokyo with the collaboration with Cadence Corporation.

References

[1] F. Grassia, L. Buhry, T. Levi, J. Tomas, A. Destexhe, and S. Saïghi, "Tunable neuromimetic integrated system for emulating cortical neuron models," *Frontiers in NEUROSCIENCE*, vol. 5, no. 134, pp. 1–12, Dec. 2011.

[2] J. Schemmel, D. Brüderle, A. Grübl, M. Hock, K. Meier, and S. Millner, "A wafer-scale neuromorphic hardware system for large-scale neural modeling," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, May 2010, pp. 1947–1950.

[3] M. Giulioni, X. Lagorce, F. Galluppi, and R. B. Benosman, "Event-based computation of motion flow on a neuromorphic analog neural platform," *Frontiers in Neuroscience*, vol. 10, no. 35, pp. 1–13, Feb. 2016.

[4] N. Qiao, H. Mostafa, F. Corradi, M. Osswald, F. Stefanini, D. Sumislawska, and G. Indiveri, "A reconfigurable on-line learning spiking neuromorphic processor comprising 256 neurons and 128k synapses," *Frontiers in Neuroscience*, vol. 9, no. 141, pp. 1–17, Apr. 2015.

[5] C. Mayr, J. Partzsch, M. Noack, S. Hänzsche, S. Scholze, S. Höppner, G. Ellguth, and R. Schüffny, "A biological-realtime neuromorphic system in 28 nm cmos using low-leakage switched capacitor circuits," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 10, no. 1, pp. 243–254, Feb. 2015.

[6] P. A. Merolla, J. V. Arthur, R. Alvarez-Icaza, A. S. Cassidy, J. Sawada, F. Akopyan, B. L. Jackson, N. Imam, C. Guo, Y. Nakamura, B. Brezzo, I. Vo, S. K. Esser, R. Appuswamy, B. Taba, A. Amir, M. D. Flickner, W. P. Risk, R. Manohar, and D. S. Modha, "A million spiking-neuron integrated circuit with a scalable communication network and interface," *Science*, vol. 345, no. 6197, pp. 668–673, Aug. 2014.

[7] V. Rangan, A. Ghosh, V. Aparin, and G. Cauwenberghs, "A subthreshold avlsi implementation of the izhikevich simple neuron model," in *Proceedings of IEEE Engineering in Medicine and Biology Conference*, Aug.–Sep. 2010, pp. 2010:4164–4167.

[8] Y. Shu, Y. Yu, J. Yang, and D. A. McCormick, "Selective control of cortical axonal spikes by a slowly inactivating k^+ current," *PNAS*, vol. 104, no. 27, pp. 11 453–11 458, Jul. 2007.

[9] H. Alle and J. R. P. Geiger, "Combined analog and action potential coding in hippocampal mossy fibers," *Science*, vol. 311, pp. 1290–1293, Mar. 2006.

[10] A. Destexhe, Z. F. Mainen, and T. J. Sejnowski, "Kinetic models of synaptic transmission," in *Methods in Neural Modeling*, 2nd ed., C. Koch and I. Segev, Eds. MA: MIT Press, 1998, ch. 1, pp. 1–25.

[11] T. Kohno and K. Aihara, "A qualitative-modeling-based low-power silicon nerve membrane," in *Proceedings of 21st IEEE International Conference on Electronics Circuits and Systems*, Dec.. 2014, pp. 199–202.

[12] ——, "Silicon neuronal networks towards brain-morphic computers," *IEICE NOLTA Journal*, vol. E5-N, no. 3, pp. 1–12, Jul. 2014.

[13] ——, "A mathematical-structure-based aVLSI silicon neuron model," in *Proceedings of the 2010 International Symposium on Nonlinear Theory and its Applications*, Sep. 2010, pp. 261–264.

[14] ——, "A design method for analog and digital silicon neurons –mathematical-model-based method–," *AIP Conference Proceedings*, vol. 1028, pp. 113–128, Jul. 2008.

[15] ——, "Mathematical-model-based design method of silicon burst neurons," *Neurocomputing*, vol. 71, no. 7–9, pp. 1619–1628, Mar. 2008.

[16] T. Kohno, M. Sekikawa, J. Li, T. Nanami, and K. Aihara, "Qualitative-modeling-based silicon neurons and their networks," *Frontiers in Neuroscience*, vol. 10, no. 273, pp. 1–16, Jun. 2016.

[17] S. Brink, S. Nease, P. Hasler, S. Ramakrishnan, R. Wunderlich, A. Basu, and B. Degnan, "A learning-enabled neuron array ic based upon transistor channel models of biological phenomena," *IEEE Transaction Biomedical Circuits and Systems*, vol. 7, no. 1, pp. 71–81, Feb. 2013.

[18] A. A. V. Hill, J. Lu, M. A. Masino, and R. L. Calabrese, "A model of a segmental oscillator in the Leech heartbeat neuronal network," *Journal of Computational Neuroscience*, vol. 10, no. 3, pp. 281–302, May 2001.

[19] R. J. Butera, Jr., J. Rinzel, and J. C. Smith, "Models of respiratory rhythm generation in the pre-Bötzinger complex. i. bursting pacemaker neurons," *Journal of Neurophysiology*, vol. 82, no. 1, pp. 382–397, Jul. 1999.

[20] X.-J. Wang, "Genesis of bursting oscillations in the Hindmarsh-Rose model and homoclinicity to a chaotic saddle," *Physica D*, vol. 62, no. 1–4, pp. 263–274, Jan. 1993.