Systematic Microwave Network Analysis for Arbitrary Shape Printed Circuit Boards With a Large Number of Vias

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***Abstract*—When calculating the admittance matrix of a singular via, a two-port microwave network is obtained instead of the three-port circuit network in the intrinsic via circuit model , without changing any accuracy. Combined with the novel impendence of a parallel plate pair; we can obtain a systematic method to analyze arbitrary shape printed circuit boards with a large number of vias.**

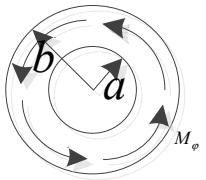
I. INTRODUCTION

The increase of integrated circuit package density results in a high concentration of interconnecting lines, which makes the use of a multilayer printed circuit boards (PCBs) become necessary. In multilayer high-speed printed circuit boards or packages, the signal traces are usually on different layers. So vias are widely used to connect the signal traces on different layers and decrease the complexity of the high-speed digital electronic systems. But as discontinuities, vias may cause a lot of signal integrity problems such as crosstalk, ring, mismatch, and mode conversion [1], [2]. Some parasitic phenomenon ignored at low frequency will become more prominent and serious impact on the interconnect performance, when the systems working at Gb/s range. Therefore an accurate model of printed circuit boards with vias is critical for high-speed digital systems.

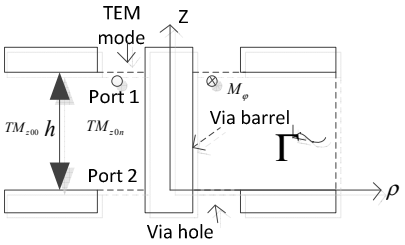
Certainly the numerical methods are generally used to address this problem. Moreover, in most of the methods the computational burden sharply grows as the size increases and the structure becomes more complex. This is the biggest limitation of the numerical methods to solve the particularly complex structure. To overcome this limitation, a physics-based via model was proposed based on physical institution in [3], [4]. In this model, each cavity of the multilayer structure is treated separately, ignoring the interaction between the different layers. In each cavity, the via-plate structure is equivalent to a π-type circuit which consists of a simple short circuit, representing the barrel of a via, and two shunt capacitors, representing the interaction between the via barrel and the top/bottom plate. Meanwhile, the plate-pair is modeled as the return current path impedance Z_{pp}.

Note that although this model offers a tremendous flexibility to model arbitrary shape PCBs, it does not satisfy the boundary conditions of the via structure rigorously.

Naturally, a more accurate and efficient method have been introduced in [5]. The intrinsic circuit model reckons in the contribution of the evanescent modes in the antipad region of vias, which is ignored in the physics-based via model. Three assumptions are proposed in the intrinsic via model, which will still be used in our work. With these assumptions, we can divide the whole plate-pair into two domain, via domain and plate domain, as shown in Fig. 1.



(a)



(b)

Fig. 1. (a) Top view of a via hole (b) side view of an irregular plate pair

The work of this paper is to first simply the three port network, the equivalent of a via domain, into two-port network. Then combined with the method to solve Z_{pp} depicted in [6], we can obtain a systematic method to analyze arbitrary shape printed circuit boards with a large number of vias.

II. SYSTEMATIC MICROWAVE NETWORK ANALYSIS

Under the first assumption in [5], we know that only $TM_{z0n}(n \geq 0)$ modes can be excited in the region between

the plate-pair when the displacement current flows through via barrel. Using the equivalence principle, the TEM mode in the via hole is represented by an angular magnetic current ring source M_φ as

$$M_\varphi = -\frac{V_0}{\rho' \ln(b/a)}\delta(z-z') \tag{1}$$

where V_0 is the voltage between the via barrel and antipad at $z'=0$ or $z'=h$.

In this paper, we do not account the effect of the pad. In other words, only the magnetic field due to the magnetic frill current distributed at the region $a \le \rho \le b$ should be considered. In [7], the expression of the magnetic field as

$$H_\varphi(a,z) = -\frac{\omega\varepsilon\pi V_0}{h\ln(b/a)}\sum_{n=0}^{\infty} G_n^s(a)\cos\left(\frac{n\pi z}{h}\right)\cos\left(\frac{n\pi z'}{h}\right) \tag{2}$$

where the auxiliary is defined as

$$\begin{aligned} G_n^s(a) = {} & \frac{\left(1-\Gamma_a^{(n)}\Gamma_b^{(n)}\right)^{-1}}{k_n(1+\delta_{n0})} \\ & \cdot\{[H_0^{(2)}(k_n b) - H_0^{(2)}(k_n a)] \\ & +\Gamma_b^{(n)}\left[J_0(k_n b) - J_0(k_n a)\right]\} \\ & \cdot\left[J_1(k_n a) + \Gamma_a^{(n)} H_1^{(2)}(k_n a)\right] \end{aligned} \tag{3}$$

where $\Gamma_a^{(n)}$ and $\Gamma_b^{(n)}$ are the reflection coefficients for the nth cylindrical waves from the via barrel and the outer radial boundary, as

$$\Gamma_a^{(n)} = -\frac{J_0(k_n a)}{H_0^{(2)}(k_n a)} \tag{4}$$

$$\Gamma_b^{(n)} = \begin{cases} -\dfrac{H_0^{(2)}(k_n b)}{J_0(k_n b)} & PEC \\ -\dfrac{H_1^{(2)}(k_n b)}{J_1(k_n b)} & PMC \\ 0 & PML \end{cases} \tag{5}$$

and k_n is the radial wavenumber of the TM_{z0n} modes as

$$k_n = \sqrt{k_0^2\varepsilon_r - \left(\frac{n\pi}{h}\right)^2} \tag{6}$$

The current due to the magnetic field distributed on the via barrel as [8]

$$\begin{aligned} I(a,z) &= 2\pi a H_\varphi(a,z) \\ &= -\frac{2a\omega\varepsilon\pi^2 V_0}{h\ln(b/a)}\sum_{n=0}^{\infty} G_n^s(a)\cos\left(\frac{n\pi z}{h}\right)\cos\left(\frac{n\pi z'}{h}\right) \end{aligned} \tag{7}$$

The admittance matrix of the equivalent two-port network can be defined as [1]

$$\begin{bmatrix} I_t \\ I_b \end{bmatrix} = \begin{bmatrix} Y_{tt} & Y_{tb} \\ Y_{bt} & Y_{bb} \end{bmatrix}\begin{bmatrix} V_t \\ V_b \end{bmatrix} \tag{8}$$

where (V_t, I_t) and $(V_b, I_b)$are the voltage and current pair of port1 and 2. The reciprocity of the material between the plate-pair results in the admittance matrix satisfies reciprocal, that is $Y_{bt} = Y_{tb}$. The admittance matrix of the two-port network can be obtained as follow:

1) Let $V_t = 0$ and $V_b = V_0$,then $I_b = I(a,0)$ and $I_t = -I(a,h)$

$$Y_{tb} = \frac{I_t}{V_b}\Big|_{V_t=0} = \frac{2\omega\varepsilon\pi^2 a}{h\ln(b/a)}\sum_{n=0}^{\infty}(-1)^n G_n^{(s)}(a) = Y_{bt} \tag{9a}$$

$$Y_{bb} = \frac{I_b}{V_b}\Big|_{V_t=0} = -\frac{2\omega\varepsilon\pi^2 a}{h\ln(b/a)}\sum_{n=0}^{\infty} G_n^{(s)}(a) \tag{9b}$$

2) Let $V_t = V_0$ and $V_b = 0$,then $I_b = -I(a,0)$ and $I_t = I(a,h)$

$$Y_{tt} = \frac{I_t}{V_t}\Big|_{V_b=0} = -\frac{2\omega\varepsilon\pi^2 a}{h\ln(b/a)}\sum_{n=0}^{\infty} G_n^{(s)}(a) \tag{10}$$

Now we have obtained the admittance of a single via. For a P-vias domain, top (bottom) voltage (current) vectors are represented as

$$\mathbf{V(I)_{t(b)}} = \left[\mathrm{V}(I)_{t(b)}^{(1)}, \mathrm{V}(I)_{t(b)}^{(2)}, \cdots, \mathrm{V}(I)_{t(b)}^{(P)}\right]^T \tag{11}$$

The admittance of the P-via network can be derived easily from the two-port admittance matrix of each via as

$$\begin{bmatrix} \mathbf{I_t} \\ \mathbf{I_b} \end{bmatrix} = \begin{bmatrix} \mathbf{Y_{tt}} & \mathbf{Y_{tb}} \\ \mathbf{Y_{bt}} & \mathbf{Y_{bb}} \end{bmatrix}\begin{bmatrix} \mathbf{V_t} \\ \mathbf{V_b} \end{bmatrix} \tag{12}$$

where

$$\mathbf{Y_{\alpha\beta}} = diag\{Y_{\alpha\beta}\} \qquad \alpha,\beta = t,h \tag{13}$$

Combine with the $\mathbf{Y_{pp}}$ obtained through the method depicted in [6], the admittance matrix of the whole plate-pair with P-vias can be derived as

$$\mathbf{Y}_{\text{final}} = \begin{bmatrix} \mathbf{Y}_{tt} & \mathbf{Y}_{tb} \\ \mathbf{Y}_{bt} & \mathbf{Y}_{bb} \end{bmatrix} + \begin{bmatrix} \mathbf{Y}_{pp} & -\mathbf{Y}_{pp} \\ -\mathbf{Y}_{pp} & \mathbf{Y}_{pp} \end{bmatrix} \quad (14)$$

Obviously, $\mathbf{Y}_{\text{final}}$ is a 2P-dimensional matrix. Then, the scattering matrix among multiple coaxial ports can be obtained as [6]

$$\mathbf{S} = \left(\mathbf{Y}_0 + \mathbf{Y}_{\text{final}}\right)^{-1}\left(\mathbf{Y}_0 - \mathbf{Y}_{\text{final}}\right) \quad (15)$$

Where $\mathbf{Y}_0$ is a diagonal matrix whose elements are characteristic admittances $0.02\Omega^{-1}$.

III. VALIDATIONS AND DISCUSSIONS

To validate the systematic method discussed above, an example of an L-shape PCB with seven signal vias, whose dimensions are shown in Fig. 2 is studied here. The relative permittivity of the dielectric between the plate-pair is 4.2 and the loss tangent is 0.02. The radii of the via barrels and the antipads are 10mils and 15mils. Port 1-7 are defined on the top of the plate-pair, while Port 8-14 are on the opposite side. The separation of plates is 10mils. Obviously, the separation of the parallel is electrically small, so the edge boundary Γ can be approximated as a PMC boundary. The results simulated by HFSS and the present method are shown in Fig. 3 and Fig .4. In the HFSS simulation, all S-parameters obtained are normalized to 50Ω.

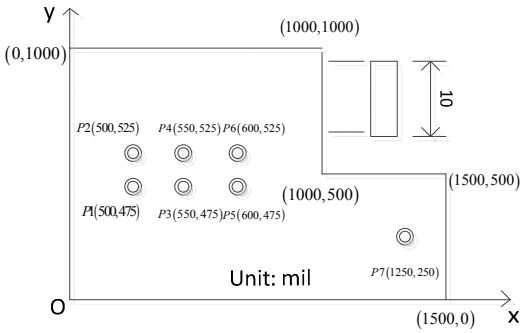


Fig. 2 Simulation model with arbitrary shape whose height is 10mils

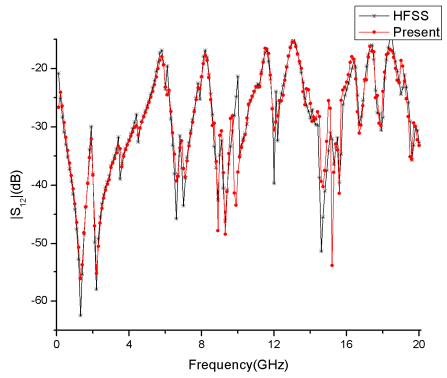


Fig. 3a Magnitude of the near-end crosstalk of the structure on the same side

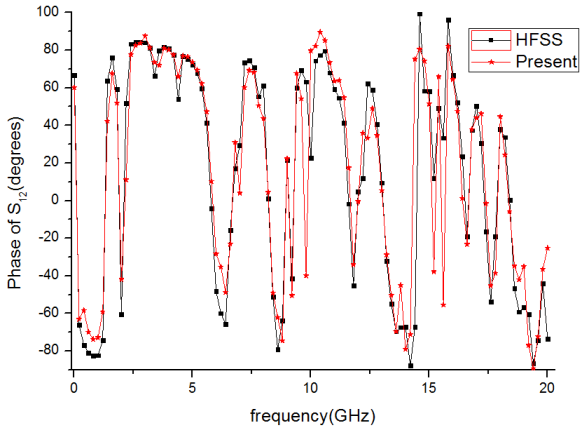


Fig. 3b Phase of the near-end crosstalk of the structure on the same side

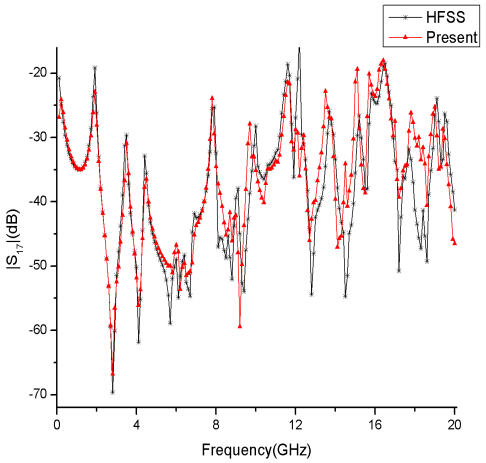


Fig. 4a Magnitude of the far-end crosstalk of the structure on the same side

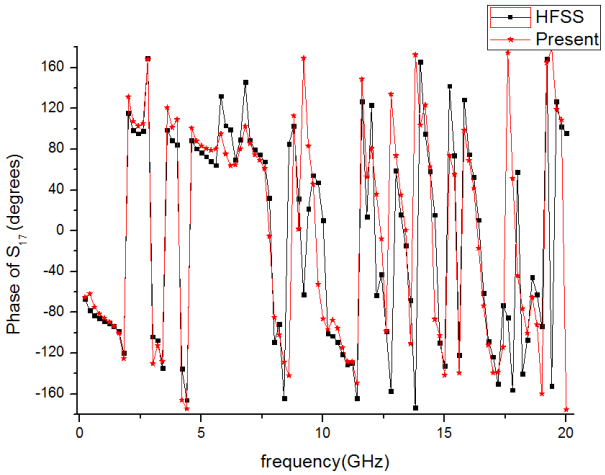


Fig. 4b Phase of the far-end crosstalk of the structure on the same side

Fig. 3a and Fig. 3b compare the magnitude and the phase of the near-end crosstalk on the same side, while Fig. 4a and Fig. 4b compare the magnitude and the phase of the far-end crosstalk on the same side. It can be seen that no matter the near-end crosstalk or the far-end crosstalk the systematic microwave network methods agrees very well

with HFSS even up to 20GHz. While the presented method can achieve such anastomosis compared with the HFSS, it only took 8min for 200 frequency sampling points instead of 2h for the HFSS simulation at the same computer, which clearly demonstrates its efficiency in modeling the arbitrary shape plate-pair with dense vias.

IV. CONCLUSION

When calculating the admittance matrix of the via domain, obviously we just need to obtain a 2P-dimensioal matrix, while 3P-dimensional matrix need to be calculated in the intrinsic via circuit model. When we calculate a via array, that is P is large, the method we presented can achieve similar accuracy, while the time spent is much less than the intrinsic via circuit model. So the method has a great potential in modeling arbitrary plate-pair structures with a large number of vias.

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