2016 International Symposium on Nonlinear Theory and Its Applications,
NOLTA2016, Yugawara, Japan, November 27th-30th, 2016

# A Switched-Current Golden Ratio Encoder Circuit 

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#### Abstract

A $\beta$-encoder is a novel analog-to-digital converter with a real number radix of $\beta$, which is robust against variations in circuit and environmental parameters. A golden ratio encoder (GRE) is a special case of the $\beta$ encoder where $\beta=\phi$ (golden ratio). This paper presents a GRE circuit based on the switched-current circuit technique. The proper operation of the proposed circuit is confirmed through numerical and SPICE circuit simulations.


## 1. Introduction

Digital circuits benefit from high density, high speed, and low power consumption and the CMOS process allows such circuits to be shrunk to a nanometer scale. On the other hand, as an interface between the analog and digital domains analog-to-digital converters (ADCs) are difficult to realize with high accuracy due to low-supply-voltage, low intrinsic gain of the advanced microfabrication transistors, and variations in component characteristics. Therefore, for example, an ADC architecture using a comparator without an operational amplifier has been proposed. However, in general, for high-performance ADC implementation, it is necessary to secure the accuracy of elements, and to introduce error correction techniques such as a digital compensation.

To alleviate these problems, a $\beta$-encoder has been proposed, which converts a real number to a digital bit sequence by using a real number radix based on the $\beta$ expansion [1,2]. One of the advantages of the $\beta$-encoder is robustness against variations in component characteristics, temperature, and noise [3, 4]. Therfore, even with circuit elements with poor characteristics in an advanced nanometer semiconductor fabrication process, it is possible to realize an accurate ADC by exploiting this robustness.

The golden ratio encoder (GRE) is a special case of the $\beta$-encoder in which the radix value is the golden ratio. It is necessary to estimate the effective radix from the output bit sequence for the $\beta$-encoder. In contrast, we can always use the fixed radix $\phi=(1+\sqrt{5}) / 2$ for the GRE. In addition, the GRE inherits all the advantages of the $\beta$-encoder.

In this paper, we propose a circuit implementation technique for the GRE. Because we aim at an integration of the GRE circuit with a low-voltage advanced microfabrication process, we employ the current-mode switched-current cir-
cuit technique. In addition, we confirm the functionality of the proposed circuit with SPICE circuit simulations and numerical simulations.

## 2. The Golden Ratio Encoder

The conversion algorithm of the GRE is given in the following:

$$
\begin{gather*}
u_{n}=\lambda_{1} u_{n-1}+\lambda_{1} \lambda_{2} u_{n-2}-b_{n}  \tag{1}\\
b_{n}=Q_{v}^{\alpha}\left(\tilde{u}_{n-2}, \tilde{u}_{n-1}\right),  \tag{2}\\
Q_{v}^{\alpha}\left(\tilde{u}_{n-2}, \tilde{u}_{n-1}\right)=\left\{\begin{array}{rr}
-1, & \tilde{u}_{n-2}+\alpha \tilde{u}_{n-1}<v, \\
1, & \tilde{u}_{n-2}+\alpha \tilde{u}_{n-1} \geq v,
\end{array}\right. \tag{3}
\end{gather*}
$$

where $x_{\text {input }} \in[-1,1]$ is the input value, $u_{-1}=x_{\text {input }}$ and $u_{0}=0$ are the initial values, $\alpha$ is the coefficient, $n$ is an integer time-index, $v$ is the threshold value of the quantizer, $b_{n} \in\{0,1\}$ is the output bit on time $n$, and $u_{n}$ is the internal state on time $n$. As shown in Fig. 1, $\lambda_{1}$ and $\lambda_{2}$ are the nonunity coefficients considering the non-ideal transfer characteristics of the delay circuits. On the other hand, the decoded analog value $\hat{x}_{\text {input }}$ from the output bit sequence can be expressed as

$$
\begin{equation*}
\hat{x}_{\text {input }}=\sum_{n=0}^{L} b_{n} \phi^{-n}, \tag{4}
\end{equation*}
$$

where $L$ is the conversion bit length.
As noted above, GRE is based on the $\beta$-encoder, and therefore, can be derived from the equation of the $\beta$ encoder with $\beta=\phi$ [3]. Taking $\phi^{2}=\phi+1$, it is possible to perform the real number expansion of the radix $\phi$ without using any multiplier unit to generate $u_{n}$. In addition, calculation of the internal state value can be constructed only with unit delay elements.


Figure 1: Representation of the non-ideal transfer characteristic of the delay elements.

### 2.1. Allowable range of threshold value $v$ and coefficient $\alpha$

Because GRE is a conversion method based on the $\beta$ encoder, variation is allowed if the threshold value $v$ and the coefficient $\alpha$ are within a certain range. If the allowable threshold values is $\delta$, i.e., $|v| \leq \delta$, and the coefficients $\lambda_{1}$ and $\lambda_{2}$ are $\lambda \in[0.9,1]$, then the mininum and maxinum allowable values of $\alpha$ are given by

$$
\begin{align*}
\alpha_{\min } & =\frac{0.854(1+\delta)}{0.618 \lambda^{2}+0.236 \lambda}  \tag{5}\\
\alpha_{\max } & =9.47-\frac{6.472}{\lambda}-\delta\left(24.8 \lambda^{2}-34.27 \lambda+11.71\right) . \tag{6}
\end{align*}
$$

## 3. Switched-Current Golden Ratio Encoder Circuit

A block diagram of the proposed switched-current GRE circuit is shown in Fig. 2. As shown in the figure, each conversion stage takes the internal state values of the previous one and two times from the other conversion stage. Then, it outputs a single digital bit, and the internal state values of the previous one and current times to the other stage as a loop. The output bit sequnce $b_{1}^{1}, b_{1}^{2}, b_{2}^{1}, \ldots, b_{L / 2}^{1}$, and $b_{L / 2}^{2}$ is obtained by repeating this loop, that is, [Stage $1 \rightarrow$ Stage $2 \rightarrow$ Stage $1 \rightarrow \cdots$ ] as many times as the bit length $L$. Figure 3 shows the conversion stage in Fig. 2, where $k=1$ and 2 . As shown in the figure, each stage is composed of a weighted 2 -input adder, a quantizer, and a 3-input adder.


Figure 2: Block diagram of the switched-current GRE circuit.


Figure 3: Block diagram of Stages 1 and 2 in Fig. 2.

### 3.1. Weighted adder circuit

The weighted adder, which is surrounded by the solid line in Fig. 3, is realized by the circuit shown in Fig. 4. In addition, Fig. 5 defines the circuit symbol of this circuit. In the circuit of Fig. 4, the relationship between input voltages $V_{i n 1}^{+}, V_{i n 1}^{-}, V_{i n 2}^{+}$and $V_{i n 2}^{-}$, and output voltages $V_{O P}$ and $V_{O M}$ are given by Eq. (7) [7].
$V_{O P}-V_{O M}=\frac{V_{A I}}{V_{A O}} \cdot \frac{\mu_{n} C_{o x}}{K_{p}}\left\{\frac{W_{1}}{L_{1}}\left(V_{i n 1}^{+}-V_{i n 1}^{-}\right)+\frac{W_{2}}{L_{2}}\left(V_{i n 2}^{+}-V_{i n 2}^{-}\right)\right\}$,
where $K_{p}=\mu_{p} C_{o x}$ is the transconductance parameter of a $p$-type MOSFET. In addition, $V_{A I}$ and $V_{A O}$ are given by

$$
\begin{align*}
V_{A I} & =V_{\text {in-cm }}-V_{\text {thn }},  \tag{8}\\
V_{A O} & =V_{D D}-V_{\text {out }-c m}-\left|V_{\text {thp }}\right|, \tag{9}
\end{align*}
$$

where $V_{\text {in-cm }}$ is the input common mode voltage, $V_{\text {out-cm }}$ is the output common mode voltage, and $V_{t h n}$ and $V_{t h p}$ are the threshold voltages of $n$-type and $p$-type MOSFETs, respectively.

In the circuit shown in Fig. 4, when $L_{1}=L_{2} \equiv L, V_{\text {in1 }}^{-}=$ $V_{i n 2}^{-} \equiv V_{i n}^{-}$, and the threshold voltage $v$ of GRE is $v=V_{i n}^{-}$, the coefficient $\alpha$ in Eq. (3) can be determined by $W_{1}$ and $W_{2}$, namely, $\alpha=W_{1} / W_{2}$. Furthermore, the coefficient $\alpha$ can be close to the golden ratio by taking two subsequent numbers from the Fibonacci sequence, that is, $1,1,2,3,5$, $8, \ldots$, so that the aspect ratios ( $W / L$ ) of MOSFETs M1 and M2 can be integers to approximate the value of $\phi$.


Figure 4: The weighted adder circuit in Fig. 3.


Figure 5: The circuit symbol for the weighted adder circuit of Fig. 4.


Figure 6: Switched-current golden ratio encoder circuit.

### 3.2. Golden ratio encoder circuit implementation

We propose a GRE circuit in Fig. 6 with the switchedcurrent technique based on the CMOS analog inverter circuit. WA1 and WA2 in Fig. 6 correspond to the weighted adder circuits of Fig. 4. In addition, CP 1 and CP 2 are the latched comparators to implement the quantizer $Q_{v}^{\alpha}(\cdot, \cdot)$ in Fig. 3.

In the switched-current circuits, capacitors for holding the sample values can be realized by the parasitic capacitances of the inverters. Therefore, the proposed GRE circuit makes it possible to miniaturize the circuit because it is mostly composed of MOSFETs without additional capacitors. Moreover, a switched-current circuit is suitable for low-power-supply voltage operation because of its small voltage swings at low-impedance nodes.

Figure 7 shows clock waveforms for driving the circuit of Fig. 6. We explain the circuit operation of Fig. 6 on the clock waveforms of Fig. 7. First, at time $t_{0}$, an input current signal is converted into voltage by inverter A1, and the current from $V_{i n-c m}$ is by A2. These voltage values are held on the parasitic capacitances $C_{g s 1}, C_{g s 2}$, and $C_{g s 3}$ of inverters A3, A4, and A5, respectively. At the same time, the converted voltage signals are applied to the weighted adder WA1. At time $t_{1}, b_{1}^{1}$ is outputted by the comparator CP1, and the outputs of Stage 1 are inputted to Stage 2. The operation of Stage 2 is similar to that of Stage 1, where the input current signals are converted into voltages by inverters A6 and A7, and they are held on parasitic capacitances $C_{g s 4}, C_{g s 5}$, and $C_{g s 6}$ of inverters A8, A9, and A10, respectively. At the same time, these voltage signals are applied to the weighted adder WA2. At time $t_{2}, b_{1}^{2}$ is outputted by the comparator CP2, and the outputs of Stage 2 are inputted to Stage 1 recurrently. This recurrent process is repeated $L$ times, where $L$ is the bit length of the ADC.


Figure 7: The clock waveforms for driving the circuit in Fig. 6.

## 4. Simulation Results

The operation of the proposed circuit was confirmed by numerical simulations and SPICE circuit simulations. In the simulations, we evaluate the return maps of the internal state, and the encode-decode characteristics.

### 4.1. Return maps

Figure 8 shows the return map of $u_{n-1}-u_{n-2}$ obtained by numerical simulation of Eqs. (1)-(3) with $\alpha=1.6$ and $v=0$. Figure 9 shows the corresponding SPICE simulation results of the proposed circuit using ideal circuit elements. From the results of Fig. 8 and Fig. 9, it can be confirmed that the overall behavior of the internal state obtained from the SPICE simulation agrees with that from the numerical simulation.

### 4.2. A/D-D/A conversion characteristic

Figure 10 shows the $\mathrm{A} / \mathrm{D}-\mathrm{D} / \mathrm{A}$ conversion (encode and decode) characteristic by the numerical simulation of


Figure 8: Return map of $u_{n-1}-u_{n-2}$ (Numerical simulation).


Figure 9: Return map of $u_{n-1}-u_{n-2}$ (SPICE simulation).

Eqs. (1)-(4) with $\alpha=1.6, v=0$, and $L=12$. Figure 11 shows the corresponding SPICE simulation results of the proposed GRE circuit. From these figures, it can be confirmed that the encode-decode characteristic of the SPICE simulation agrees with that of the numerical simulation. Hence, it is confirmed that the proposed switched-current GRE circuit faithfully implements the GRE equations.

## 5. Conclusion

We have proposed the GRE circuit based on the switched-current circuit technique with the analog CMOS inverter circuit. The operation of the proposed circuit was confirmed by numerical and circuit simulations.

## Acknowledgment

This work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc.

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Figure 10: A/D-D/A conversion characteristic (Numerical simulation).


Figure 11: A/D-D/A conversion characteristic (SPICE simulation).
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