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Extremal optimisation approaches for building complex geometric structures in 3D integrated circuits

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Abstract—The 3D integrated circuit design task poses an extremely difficult intellectual challenge. Modern integrated circuits are composed of thousands of buildingg blocks and billions of transistors. Also an additional challenge is posed by realisation of various blocks using heterogeneous technologies such as CMOS of various technology nodes, batteries and super capacitors, sensors, RRAM memories and many others. Solution of the extremely difficult problem of building block geometric positioning and their interconnects. The solution has to meet a number of specific requirements and satisfy a variety of constraints. Efficient search of huge and discontinuous solution spaces requires new non-deterministic and heuristic algorithms. The goal of our research is to minimize the total wirelength of interconnects between sub-circuits. The paper presents a knowledge intensive 3D ICs layout hypergraph representation together with the elaborated neighborhood optimization heuristics. The results of the Extremal Optimization (EO) implementation applied to the MCNC set of benchmark circuits are reported.