Design and Analysis of Flexible Interconnects on an Extremely Thin Silicon Substate for Flexible Wearable Devices

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***Abstract*—In this paper, we designed, fabricated and analyzed the microstrip line structure flexible interconnects on an extremely thin silicon substrate for future flexible wearable devices. The electrical characteristics of a flexible silicon chip and a PCB are analyzed when mechanical structural changes. The fabricated flexible chip is attached on the flexible PCB using elastic polymer bumps. By using the fabricated flexible chip and PCB, S-parameter of the interconnects were measured with the bending radius until the flexible chip is disconnected from the PCB. As the results, the designed flexible chip on the flexible PCB showed the resonance peaks when the bending radius is less than 10 mm. Moreover, the interconnection between the chip and PCB is fully disconnected when r is less than 7.5 mm.**

Keywords— flexible chip, flexible interconnects, flexible PCB, signal integrity, S-parameter, thin silicon substrate

I. INTRODUCTION

Recently, flexible electronics are becoming popular due to its specificity. These electronics can be applied to a human body with the higher flexibility. Many electronic products such as smartphone, smartwatch, and internet of things (IoTs) have been released with the flexible shape [1]-[3]. However, in the existing products, the most of electronic circuits were implemented in a rigid part of the device. To implement the electronic circuits in a flexible part of the device, a printed circuit board (PCB), bumps, and a silicon chip must be flexible. Generally, the thickness of a silicon substrate is larger than 100 μm and it is brittle. To have the flexibility, the silicon substrate must have the thickness less than 50 μm. In this case, the chip can be bent without the cracks.

As the system operating frequency increases, it is essential to design the signal channels carefully. In high-speed channels, signal degradation, coupling between the channels, and electromagnetic interference (EMI) are the important issues [4]. Moreover, for the flexible chips, the electrical characteristics of the channels can be changed due to mechanical stress and fatigues by the repetitive bending. Therefore, we have designed the flexible interconnection lines with the extremely thin flexible silicon substrates to analyze the interconnects with the mechanical bending. Fig. 1 shows the designed flexible interconnection lines on the flexible PCB. The flexible chip is attached on the flexible PCB using the polymer bumps [5]. The thickness of the silicon substrate is 12.6 μm to have the flexibility. The polymer bumps are elastic bumps that reduces the mechanical stress. The material of the PCB is polyimide that has good electrical and thermal characteristics [6].

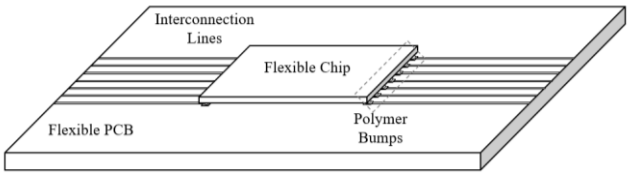


Fig. 1. The structure of the designed flexible chip on the flexible PCB. The flexible chip is attached on the PCB with the polymer bumps.

II. DESIGN AND FABRICATION OF FLEXIBLE CHIP AND PCB WITH MICROSTRIP INTERCONNECTION LINES

A. Design of the Flexible Chip and PCB with Interconnects

The 4 mm interconnection lines on the flexible chip were designed with the HFSS 3D EM simulation tool considering the 50 ohm characteristic impedance of themicrostrip line structure. The designed thicknesses of the flexible chip are listed in TABLE I. For the silicon substrate, the silicon wafer is grinded to 12.7 μm. For the oxidation layer, it has 0.3 μm thickness. For the copper layer such as the interconnection lines and a ground plane, they have 2.5 μm of the average thickness. The thickness of the dielectric layer between the interconnection lines and the ground plane is 11 μm with relative permittivity of 3.5. Finally, the polymer bumps have the thickness of 20 μm before mechanical stress is applied. The total thickness of the flexible chip is less than 50 μm excluding the polymer bumps.

TABLE I. THICKENESS OF THE DESIGNED FLEXIBLE CHIP

	Silicon Substrate	Oxidation Layer	Copper Layer	Dielectric Layer (e_r=3.5)
Thickness (μm)	12.6	0.3	2.5	11

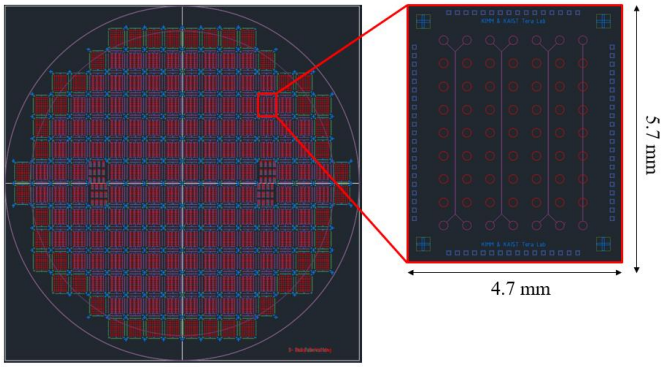


Fig. 2. Designed the flexible interconnection line using a CAD tool with the dimension of the single chip. The interconnection line is designed with the microstrip line structure.

(a) (b)

Fig. 3. The fabricated flexible wafer from KIMM. The fabricated silicon wafer is grinded to achieve the silicon substrate thickness of 12.6 μm. (a) After back grinding. (b) After dicing the wafer.

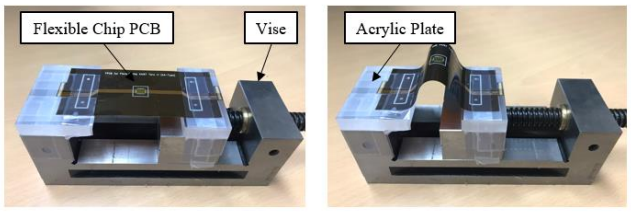
TABLE II. THICKENESS OF THE DESIGNED FLEXIBLE PCB

	Polyimide Coverlay	Copper Layer	Polyimide Substrate
Thickness (μm)	12.7	17.5	38.1

Fig. 2 shows the designed the interconnection line using a CAD tool. The 4-inch wafer is used to design the chip. Total 150 chips can be fabricated from a single wafer. For the flexible PCB, the polyimide substrate is used. The thickness of the flexible PCB is given in TABLE II. The thickness of the each layer in the PCB is chosen as thin as possible by considering the PCB manufacturing process. The microstrip interconnection line on the PCB has total length of 125 mm with 50 ohm characteristic impedance. For the PCB, we achieve the total thickness of 150 μm including adhesive layers.

B. Fabrication of the Flexible Chip with the Microstrip Interconnection Line

The designed chip is fabricated by Korea Institute of Machinery and Materials (KIMM) as shown in Fig. 3. Before dicing of the wafer, the silicon wafer is grinded to achieve the target thickness of 10 μm. After the grinding, the actual thickness of silicon wafer was 16.5 μm. Moreover, after the chemical-mechanical planarization (CMP) process, we could achieve the silicon wafer thickness of 12.6 μm.



(a) (b)

Fig. 4. The measurement jig of the flexible chip and PCB. The vise is used to bend the flexible chip. To avoid signal degradations by the metallic effect of the vise, the acrylic plate is used. (a) The flexible chip without the bending. (b) The flexible chip with the bending.

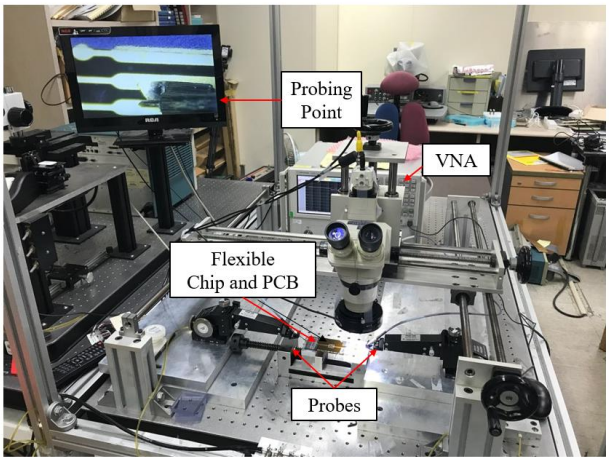


Fig. 5. The measurement setup of the flexible chip. The probe station and vector network analyzer (VNA) is used to measure the insertion loss (S_{21}) of the flexible interconnection lines.

III. MEASUREMENT OF THE FLEXIBLE CHIP ON THE PCB WITH THE MECHANICAL BENDING

A. Measurement Setup of the Flexible Chip

To measure the flexible chip with the bending, we have attached the flexible chip on the PCB using the polymer bumps and non-conductive adhesive film (NCF). Fig. 4 shows the measurement jig of the flexible chip and PCB. The vise is used to bend the flexible chip. The acrylic plate is used to avoid any signal degradation due to the metallic effect of the measurement vise. Fig. 4 (a) shows the flexible chip without the bending when the chip and PCB were flat. Fig. 4 (b) shows the flexible chip when we apply the mechanical bending.

Fig 5 shows the measurement setup of the flexible chip. To measure the insertion loss (S_{21}) of the interconnection lines in the flexible chip, a vector network analyzer (VNA) is used. In addition, to measure the flexible chip, 400 um pitch GS probe is used to reduce parasitic components from a cable and a

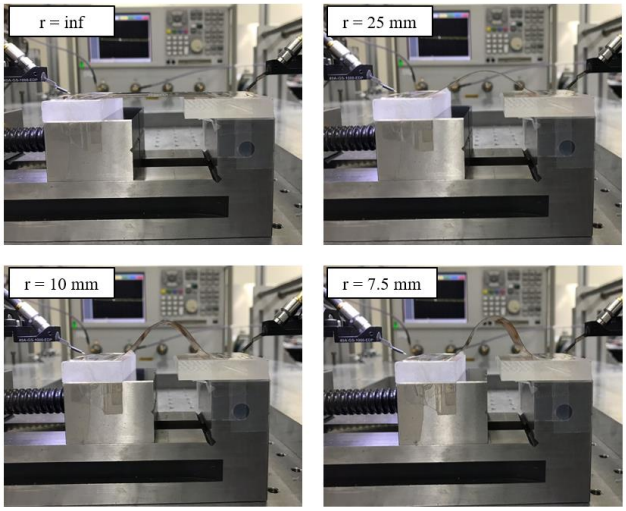


Fig. 6. The measurement setup with the bending radius of infinity, 25 mm, 10 mm and 7.5 mm.

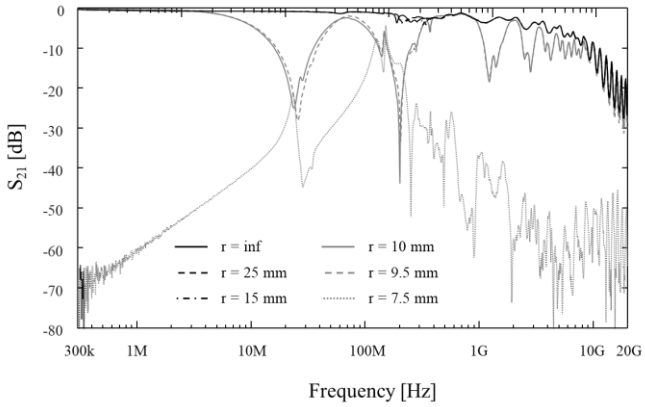


Fig. 7. S_{21} measurement results of the flexible chip and PCB with the bending radius. When bending radius r is 10 mm, the resonance is occurred. and when r is 7.5 mm, the results showed the open connection.

connector. Finally, for the frequency set up, we measured it from 300 kHz to 20 GHz. Fig.6 shows the measurement setup with the bending radius of infinity, 25 mm, 10 mm and 7.5 mm respectively.

B. Measurement Results with the mechanical bendings

Fig. 7 shows the measurement results of the flexible chip with the bending radius r. When r is infinite, the resonance is produced over 1 GHz range. This resonance is produced by the impedance mismatching between the chip and PCB. Once we apply the bending radius from infinite to 15 mm, the insertion loss characteristics have not affected. S_{21} remained until r becomes 10 mm. When r is reduced to 10 mm, S_{21} is affected and the resonances at several frequencies were produced. Finally, when r is 7.5 mm, the result showed that the flexible chip and PCB are fully disconnected.

Finally, we found that the designed flexible chip and PCB have the minimum bending radius of 7.5 mm. If we apply the

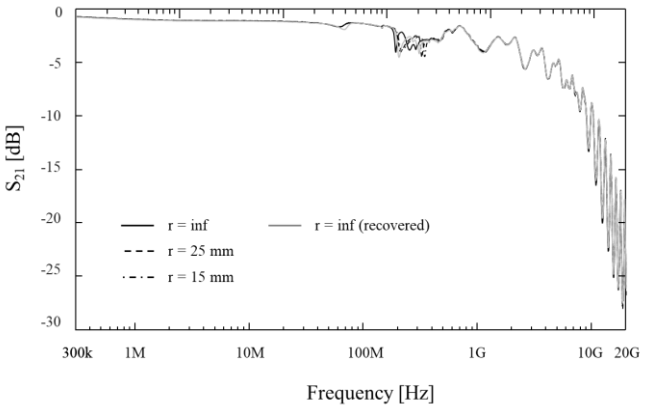


Fig. 8. S_{21} measurement results of the flexible chip and PCB when the r is increased again from 7.5 mm to infinite. The result shows that the S_{21} result of the flexible chip and PCB is also improved to original S_{21} result.

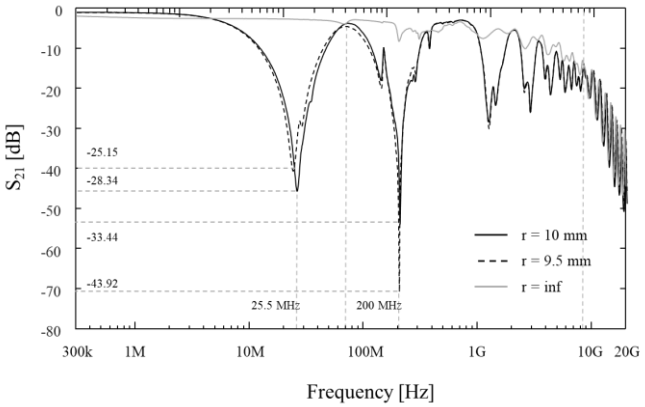


Fig. 9. S_{21} measurement result of the flexible chip and PCB with the bending radius between 10 mm and 9.5 mm. When the bending radius is less 10 mm, we could observe the resonance peaks at 25.5 MHz and 200 MHz.

smaller bending radius than 7.5 mm, the signal cannot be transmitted. After the disconnection between the chip and PCB, we have increased the bending radius of the flexible chip from 7.5 mm to infinite to see whether the chip and PCB are reconnected or not. The light solid line in Fig. 8 shows the S_{21} result when we increase the bending radius to infinite. As the result, we can see that the S_{21} result of the flexible chip is improved again to original S_{21} result.

Fig. 9 shows the S_{21} results of the flexible chip and PCB with the bending radius between 10 mm and 9.5 mm. When the bending radius is less than 10 mm, we could observe the resonance peaks at 25.5 MHz and 200 MHz. When r is 10 mm, the resonance peaks have S_{21} value of -28.34 dB and -33.44 dB respectively. When r is 9.5 mm, S_{21} of the resonance peaks become -25.15 dB and -43.92 dB respectively. As we decrease the r value, the resonance peak at 25.5 MHz was slightly improved. However, at 200 MHz, the S_{21} result becomes worse. If the system operating frequency and those resonance frequencies were similar, the signal will be degraded critically due to large insertion loss and reflections. This can be a serious challenge for the flexible packages.

IV. Discussions

In this paper, we have designed the flexible chip and PCB for future wearable device interconnection scheme. By using the fabricated flexible chip and PCB, we have measured the insertion loss (S_{21}) as we apply the bending radius from infinite to 7.5 mm. Until we reduce the bending radius from infinite to 10 mm, we could not observe any changes in S_{21}. However, when r less than 10 mm, we could observe the resonance peaks. This resonance peak is produced due to gaps between the chip and PCB as mechanical stress is applied. Since the lower frequency region has similar trends for S_{21}, the resonance effect cannot be detected from lower frequency analysis or DC resistance. Therefore, wide band frequency analysis is required.

In addition, when r becomes 7.5 mm, the S_{21} result showed the open connection between the interconnects. This means when r is less than 7.5 mm, the polymer bumps will be completely disconnected from the flexible chip or PCB. However, most of the wearable devices will have a surface with the bending radius greater than 7.5 mm. Moreover, in this paper, the flexible chip is not molded and it is purely bonded with the non-conductive adhesive film (NCF). By choosing the proper molding materials, we can reduce the stress on the flexible chip by reducing the young's modulus around the flexible chip. This will enable the flexible chip to apply on the flexible wearable devices with the smaller bending radius.

V. Further works

For the further research, we will use the molding materials to reduce the mechanical stress on the flexible chip. This will reduce the bending radius r and improve the reliability of the flexible system. Moreover, not only the passive interconnection lines, active circuits such as power electronic and RF circuits with the mechanical bending will be analyzed.

VI. Cnclusions

In this paper, we have designed, fabricated and analyzed the microstrip line structure flexible interconnects on a silicon substrate. We have attached the flexible chip on the flexible PCB to analyze any electrical characteristic changes as we apply the mechanical stress. We applied the mechanical bending to the flexible chip on the flexible PCB and we measured the insertion loss (S_{21}). As the result, when the bending radius r is larger than 10 mm, S_{21} result was remained. However, when r is less than 10 mm, we have observed the resonances at 25.5 MHz and 200 MHz due to the gap between the flexible chip and PCB. Moreover, when r is less than 7.5 mm, the flexible chip is fully disconnected. Finally, we conclude that our designed flexible chip and PCB have minimum bending radius of 7.5 mm.

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