Design Technique on Reduction of Power Cross Regulation and Coupling in Data Center Microprocessor Power Design

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Abstract--An analytical dual power rail simulation methodology is essential for evaluating cross regulation issues in core power designs with low-cost and multilayer printed circuit boards (PCB). With conventional validation approach, the cross regulation is a combinative result of complex power delivery networks (PDNs) and the performances of voltage regulators. Meanwhile, the measurements are usually not informative and inefficient to distinguish the root cause and help designers come up with an improvement plan. Fortunately, the analytic approach makes it possible to find the layout issues that could lead to serious cross regulations. With the analytic approach, the cross regulation problem can be simplified and modeled with distributed power delivery networks. The analytical predictions on cross regulation from power delivery impedance are more intuitive from the distributed power delivery networks. In this paper, this approach is further extended to compare two different layout schemes. Engineering implications on reducing the cross regulation in a multi-layer PCB will be discussed through a series of simulation examples.

Keywords—power delivery network; voltage regulator; cross regulation;

I. INTRODUCTION

With the demand of large and fast load transient step from central processing unit in data center platforms, the power designs have become more and more challenging with layer and area reduction in printed circuit boards (PCBs). Consequently, power cross regulation issues will become increasingly important from the perspective of power delivery and power integrity. The cross regulation, which is able to couple to other power rails easily through the power delivery networks, can collapse other rails and result in system mal-functions. It may also cause electrical over-stress or burnt issue in the device and reduce the reliability of a server. Designing a couple-free power delivery network has become a major challenge in high-speed PCB and high power CPU designs.

Despite the full wave simulators which utilize finite-difference time domain method have been used to model power-to-power or power-to-signal coupling issues. In addition, there are a lot of modeling methods that simplify the issue into 2-D structure and decomposed the parasitic and into lumped circuit or transmission lines. Another equivalent circuit based on the finite element method uses the bedspring-like network to model plane pair structure. However, these methods have difficulties in modeling multiple plane structures. Recently, a multilayer finite difference method (FDM) has been proposed, which extends the FDM method to multiple plane structures. They usually provide accurate results but are also computation-intensive and lack of the influence coming from voltage regulators. Fortunately, for the cross regulation problem, the power delivery network makes the frequency of interest to tens of MHz and the applied load current does not generate high frequency noise thus make it easy to be modeled in circuit level. Based on this feature, the cross regulation modeling can be simplified with distributed power delivery network by the use of simulation program.

This paper represents a modeling and formula to analyze cross regulation issues between two power rails. The major contribution of this paper can be summarized as following items:

1) The root cause analysis and formula development for multilayer power/ground planes with switching voltage regulator(VR) behaviors;

2) The simulation result of changing coupling effect and VR responses.

II. CROSS REGULATION BETWEEN TWO POWER RAILS

With the demand of high density PCBs, it is challenging for power design and power integrity engineers to analyze the impact of cross regulation with multi-layer PCBs because of the modeling complexity and different aspects that caused the cross regulation. A cross regulation problem can be observed within two power rails that interact in the same PCB. For modern power designs in data center, CPU draws a huge

amount of current and caused a high di/dt in its power delivery network. It could easily lead to the collapse of another power rail and cause the device mal-functions. A conceptual illustration can be shown in Fig.1.
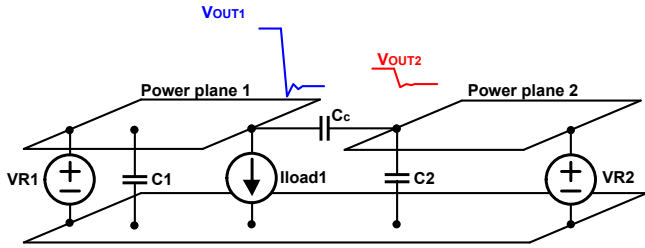

Fig.1. Conceptual cross regulation.

In Fig.1, the power rail 1 is composed of VR1, which includes the Pulse-Width Modulator controller (PWM), power stages, C1, which represents the bulk and decoupling caps, and the power/ground planes. The Iload1 is the loading current on the power rail 1, for the high performance computing demand in data center, Iload1 usually features high slew rate over than 800A/μs and large load step which is more than 200A. The coupling capacitor, Cc, which represents the effect of power plane overlaps, can couple the noise when rail 1 is under load transient. The shared ground plane can shift the voltage seen by rail 2. The response of the voltage regulator is also a factor that impacts on the cross regulation. The different response of voltage regulator 1 can generate different level of transient response on the load side. When a noise is coupled to the load side and remote sensed by the voltage regulator 2, it is supposed to be relieved by the regulation capability of VR2.
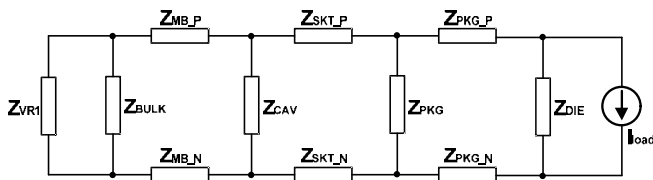

Fig.2. Typical Processor Power Delivery Network

A power delivery network of the core power rail is composed of the impedance of VR and bulk capacitors. Thru the mother board power plane then reach to the cavity capacitors. At the socket side, the CPU is with package capacitors then go into the die package. Modeling the two-sided circuit makes us easier to distinguish the effect from power planes or ground planes.

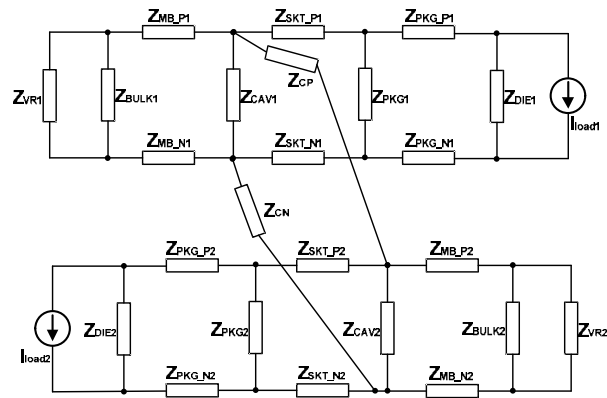The cross regulation can be modeled further as Fig. 3.

Fig.3. Cross regulation Model

The simplified equivalent circuit for transfer impedance Z_{21} can be shown in Fig. 4.

It can be derived that:

$$Z_{EQ1} = \left(Z_{VR1} \parallel Z_{BULK1} + Z_{MB_{P1}} + Z_{MB_{N1}}\right) \parallel Z_{CAV1} \parallel \left(Z_{SKT_{P1}} + Z_{SKT_{N1}} + Z_{PKG1} \parallel \left(Z_{PKG_{P1}} + Z_{PKG_{N1}} + Z_{DIE1}\right)\right)$$

$$Z_{EQ2} = \{[\left(Z_{VR2} \parallel Z_{BULK2} + Z_{MB\_P2} + Z_{MB\_N2}\right) \parallel Z_{CAV2} + Z_{SKT_{P2}} + Z_{SKT_{N2}}] \parallel Z_{PKG2} + Z_{PKG_{P1}} + Z_{PKG_{N1}}\} \parallel Z_{DIE1}$$

The transfer impedance can be derived as:

$$i = \frac{Z_{EQ1}}{Z_{EQ1} + Z_{EQ2} + Z_{CP} + Z_{CN}} \cdot (-I_1)$$

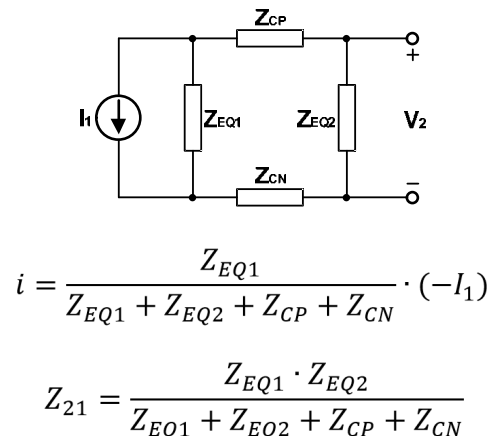$$Z_{21} = \frac{Z_{EQ1} \cdot Z_{EQ2}}{Z_{EQ1} + Z_{EQ2} + Z_{CP} + Z_{CN}}$$

Fig.4. Deviation of transfer impedance

From the transfer impedance equations, we can sweep the coupling capacitor from zero to 100pF and understand the plane to plane coupling with reasonable coupling orders. From Fig. 5, it can be observed that the rail 2 voltage can be coupled when a fast transient applied on rail 1 with different coupling effect, that is, different Z_{CP} values. In real cases, the coupling effect is conducted by multilayer PCBs, which have multiple power plane overlapping. It is straightforward to extract the capacitance caused by power plane overlapping.
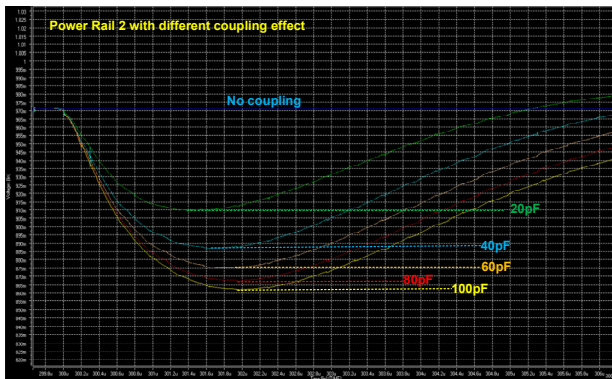
Fig.5. Different power plane overlapping with different cross regulation levels.

Secondly, we changed different GND plane layout styles, and observe different ground bounce caused by power rail 1. It can be observed from equation that with smaller Z_{EQ1}, the transfer impedance will be smaller. Therefore to enhance the ground plane or adding more layer to reduce the ground impedance can help to alleviate cross regulation. The trend can be shown in Fig. 6.
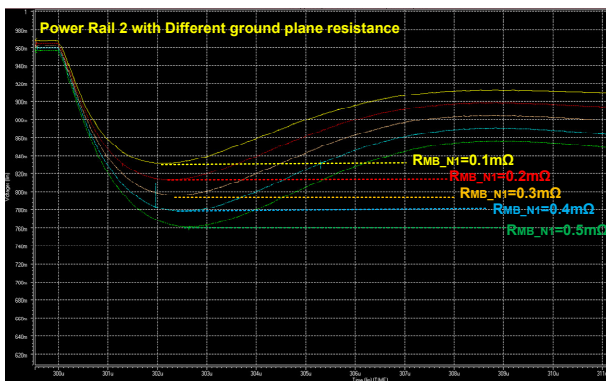

Fig.6. Different power plane overlapping with different ground plane resistance.

It is interesting that to change the voltage regulator of power rail 1 can also have impacts on the cross regulation behavior. The power designer often adjust the cavity capacitors based on the power rail 1 performance and ignored the impact on power rail 2. It can be observed either from equations or parameter sweeping of Fig. 7 and Fig. 8 to understand this trending.
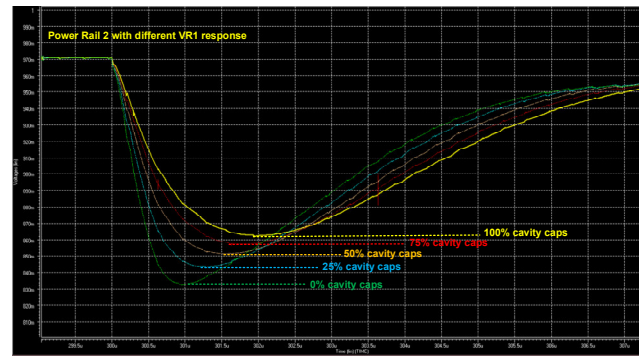

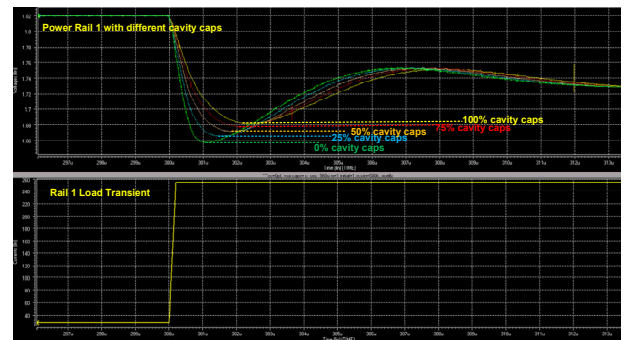Fig.7. Different power rail 2 coupling with VR1 response.

Fig.8. Different VR1 droop with respect to cavity caps.

The Z_{EQ2} is decided by the power delivery network seen by rail 2. Power engineers often focus on re-spin the layout and reducing power plane overlappings and neglect the cross regulation can be eliminated by enhance the response of voltage regulator. Fig. 9 shows different cross regulation results with different rail 2 response. With changing the switching frequency, the higher switching frequency means better response and smaller Z_{EQ2}c. The real cross regulation improvement is shown in Fig. 10.
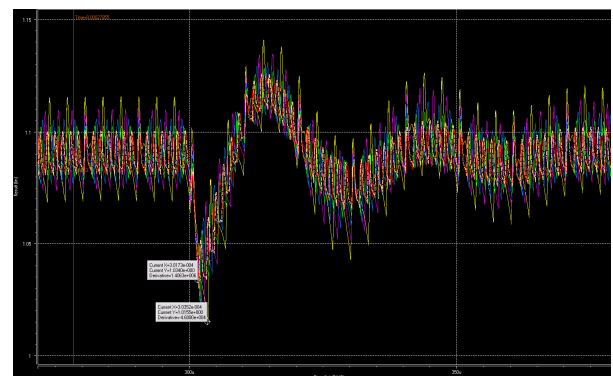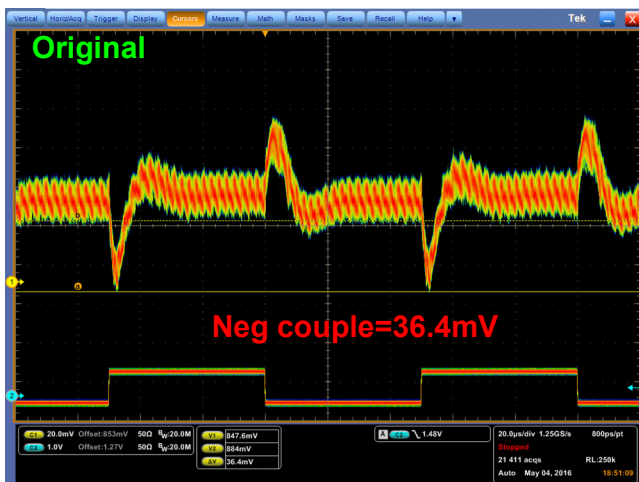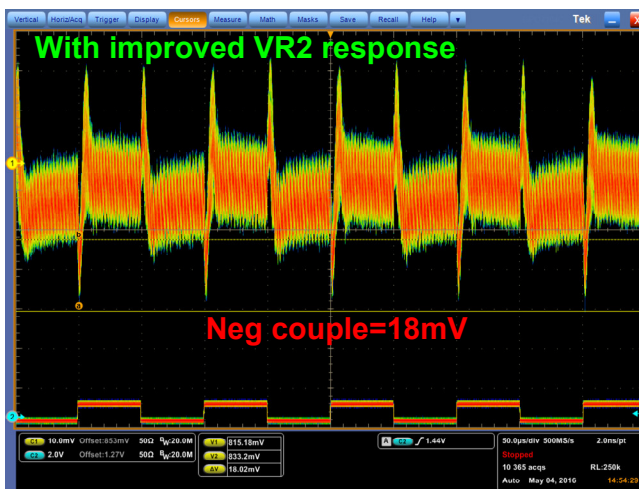

Fig.9 Different cross regulation with respect to different VR2 switching frequencies.

(a)

(b)

Fig.10 (a) Original cross regulation caused 36.4mV droop in VR2. (b) Reduction on cross regulation in a real system by enhancing VR2 response.

III. CONCLUSION

We have demonstrated a power integrity simulation methodology and analytical formula to analyze the cross regulation issues in core power designs. With derived equations, it can be easily decided what solution is helpful to reduce the cross regulations. Meanwhile, the swept waveforms is consistent with empirical solutions made by power engineers. To achieve a good transient performance without cross regulation, the power plane overlapping and power delivery networks of cross regulation shall be used to breakdown the root causes. It also provides good insights for power engineers and help to understand the requirement inside processor power designs.

REFERENCES

[1] Tsu-Wei Tseng, Chang-Tzu Lin, Chia-Hsin Lee, Yung-Fa Chou and Ding-Ming Kwai, "A power delivery network (PDN) engineering change order (ECO) approach for repairing IR-drop failures after the routing stage," VLSI Design, Automation and Test (VLSI-DAT), 2014 International Symposium

[2] Junxia Ma, Tehranipoor, M., Sinanoglu, O. and Almukhaizim, S., "Identification of IR-drop hot-spots in defective power distribution network using TDF ATPG," Design and Test Workshop (IDT), 2010 5th International

[3] Lee, J., Narayan, S., Kapralos, M. and Tehranipoor, M., "Layout-Aware, IR-Drop Tolerant Transition Fault Pattern Generation," Design, Automation and Test in Europe, 2008

[4] G. Ouyang, K. Xiao, W. Xu, J. He, J. Fang, G. Tian, X. Ye, Y. Ren, Y. Li, P. Li, "Switching voltage regulator noise coupling to connector signal pins through near field radiation", 2014 IEEE EMC symposium

[5] G. Ouyang, X. Ye and T. Nguyen, "Switching voltage regulator noise coupling to signal lines in a server system," 2010 IEEE EMC symposium