# Copper Treatment Investigation on High Frequency PCB Electrical Characteristics

Jay Lin Elite Material Co., Ltd Taoyuan, Taiwan jay.lin@mail.emctw.com

Abstract—With the increasing of transmission speed over 10GHz in telecom industry, the design possibilities are concerned and explored to lower channel loss and enhance signal integrity. In general, insertion loss comprises the sum of conductor loss and dielectric loss. The lower loss dielectric material with the smooth copper are widely adopted in the laminated printed circuit board (PCB) to reduce the loss for high frequency application. In terms of the conductor loss, how to control the copper roughness surrounded signal trace is very important to reduce the loss when the frequency is higher. These factors that affect the surface roughness are the inherent roughness of the foil itself and the surface treatment induced roughness intended to enhance innerlayer adhesion. In this paper, a study of two copper foil types with different surface treatments in ultra low-loss material is conducted to investigate the copper treatment impact on the insertion loss up to 40 GHz. The non-etching copper treatment with the smoothest roughness showed the best electrical performance among these three surface treatment approaches.

#### Keywords-conductor loss; surface treatment; signal integrity

# I. INTRODUCTION

It has been well known that conductor surface roughness can affect the conductor loss when the frequency is going higher because current flow is inhibited on the surface that we called skin effect can be estimated with the equation below (1)

$$\delta = \sqrt{\frac{1}{\pi \cdot f \cdot \mu \cdot \sigma}}$$

where  $\delta$  is the skin depth (m), f the frequency (Hz),  $\mu$  the magnetic permeability (H.m-1) and  $\sigma$  the electrical conductivity (S.m-1) of the material (copper). Around 98% of the current flow at a distance of four times the skin depth. Table 1 is the skin depth of copper and it is within the micrometer range when the frequencies is higher than 4 GHz.

(1)

Table I. Calculation of skin depth in copper depending on the frequency

Signal Frequency	Skin depth of copper
1 MHz	65 μm
1 GHz	2.1 μm
10 GHz	0.65 µm
50 GHz	0.29 μm

#### Copyright © 2019 IEICE

Jimmy Hsu Intel Microelectronics Asia Ltd., Taiwan Branch Taipei, Taiwan jimmy.hsu@intel.com

Typically, the roughness (face interior side) of electrodeposited (ED) copper foil can be up to 8um in depth, while the exterior of the foil may be quite smooth. The next level copper foil, Reverse-Treated Foil (RTF) has been widely used in mid-loss laminates and both sides of this copper foil have smaller-sized "teeth".

In addition to the two above mentioned types, some newer copper foils in the market aimed specifically at loss reduction are offered on certain ultra low-loss laminate systems. These are variants of ED foil with smaller average tooth sizes, and their proprietary designations are HVLP (Hyper Very Low Profile), as well as HVLP2 with smoother roughness. The roughness of these different copper foil types are measured by contact profilometry as shown in Table II.

	Table II. Roughness of different copper foil type
--	---

Copper Foil Type	Matte side Roughness Rz (μm)		
Standard ED	< 8		
RTF	< 3.5		
HVLP	< 2.0		
HVLP2	< 1.5		

Besides the roughness of the native copper foil, the copper oxide treatment prior to lamination process is very important for PCB manufacture process and electrical performance. Adhesion between copper conductors and insulation materials is a critical factor to ensure the reliability of PCB products. Generally speaking, conventional copper surface treatment such as oxide alternative has been widely applied in PCB industry and this approach by roughing surface will degrade the signal integrity in high frequency. Hence, non-etching type surface treatment was proposed and developed [2-3] for the adhesion. This kind of the enhanced adhesion ability with the specific chemical bonding can not only maintain of physical bonding mechanism but also improve signal integrity.

In this paper, the design experiment of two copper foil types with different copper treatments were conducted to investigate the impact on PCB electrical performance. The insertion loss is attributable to roughness of inherent matte side and applied surface oxide treatment. The measured frequency is up to 40 GHz to observe the loss changes depending on the increased frequency.

# II. ELECTRICAL CHARACTERIZATION

## A. De-embedding Metrology

Measurement methodology is one of the most important factors to characterize PCB material properties. In the IPC test method document [4], a list of loss measurement methods are described. Vector Network Analyzer (VNA) has been the standard instrument for the accurate loss measurement for a wide frequency range and many metrologies have been proposed for PCB loss characterization in the industry, including the thru-reflect-line (TRL), automatic fixture removal (AFR), smart fixture de-embedding (SFD) and etc. All de-embedding methods require additional de-embedding structure(s) other than the device under test (DUT) with fixtures. Meanwhile, de-embedding is critical for the accuracy of interconnect measurement. In the computer system design community, a cost-effective and simple measurement method with the good accuracy is preferred. To balance the cost, complexity, and accuracy, a method named Delta-L is adopted for the PCB material characterization to effectively remove the unwanted effect, such as via transition [5-6]. For the higher frequency over 20 GHz application, the test fixture design was enhanced accordingly, including launch pad optimization, probing pitch reduction from 1.0 mm to 0.5mm, more surrounding ground vias for the better current return path and etc.

Delta-L uses two different routing structures for the stripline with the vias as shown in Figure 1. The reference is the short routing "B" with the length of X2 inch and the other is the longer routing "A" with the length of X1 inch. Through Eigenvalue algorithm of Delta-L, the structure A is deembedded by B with the vias, probing contact and launching effect being de-embedded. Meanwhile, the physical fitting was applied with root omega method for the better measurement result reading.



Fig. 1. Delta-L Routing

# B. Test Vehicle Design

Besides material electrical characteristic itself, stack-up design plays an important role of the insertion loss. In this study, one specific stack-up with 4 mil core and 4.1 mil prepreg was used and the trace width and spacing are 6.25 mil and 6.5 mil, respectively, to achieve the differential impedance of 85 ohms as shown in Fig. 2. The routing length of DUT and de-embedding structure are 10 inch and 5 inch, respectively.



Fig. 2. PCB Stack-up

#### C. Measurement Configurations

In order to ensure PCB samples have the less environmental impact, it is good to have the pre-condition process before the electrical measurement. In this study, the temperature is controlled with  $23 \pm 2$  °C and humidity of  $40 \pm 5\%$  RH over 48 hours. Measurement environment is based on IEC 60068-1. The temperature is controlled from 15°C to 35 °C and the humidity is within 45~75 % RH. The measurement process need to complete the measurement within 2 hours after precondition for sample quality. IF bandwidth of Vector network analysis is set to 1 kHz and the frequency range is from 10MHz to 40 GHz with 4000 sampling points.

# D. Copper Foil and Surface Treatment

To investigate the loss resulted from copper surface treatment and copper foil type, the rest of factors such as dielectric material and PCB manufacturing conditions should be fixed.

Ultra low-loss material named Elite 8K[7] with dissipation factor of 0.0025 at 10 GHz is used as base material for each surface treatment test. The copper foil weight and types are one ounce with two copper types : HVLP and HVLP2 are adopted as inner-layer conductor. HVLP2 was observed finer grid size and smoother profile at matte side by scanning electron microscope (SEM) inspection as shown in Fig. 3.



Fig. 3. HVLP & HVLP2 copper foil (1oz) matte side by SEM x10k

For PCB manufacturing process consistency, all test boards are produced in the same time besides copper surface treatment to reduce the variance of line width and dielectric thickness.

#### Copyright © 2019 IEICE

Furthermore, to compare the influence against various roughness surface treatment, conventional oxide alternative, low-etching, and non-etching type chemical were used in this study and the surface topography after different surface treatments were also captured by SEM in Fig. 4. Non-etching type chemical without passing etching process is the smoothest one among these surface treatments.



Fig. 4. Differe surface treatment by SEM x10k

A total of four combinations of the copper foils with different surface treatment were prepared as well as the roughness parameter SRz was measured by optical surface profilers (ZygoNewView8200) in Table III. SRz is the average radial peak-to-valley areal roughness and the average of the largest half of many individual Rz results determined by slicing the areal data array about its center through 360 degrees. The Rz results are sorted by magnitude and SRz is calculated by averaging the largest 50% of the Rz values.

Table III. Test combination of copper foil and surface treatment	Table III.	Test combination	of copper	foil and	surface	treatmen
--	------------	------------------	-----------	----------	---------	----------

Sample Code	Copper Foil	Matte Side Roughness SRz(μm) Surface Treatment		Surface Roughness SRz(µm)
А	HVLP	0.60 Oxide Alternative		1.17
В	HVLP2	0.45	Oxide Alternative	1.17
С	HVLP2	0.45	Low- Etching	0.67
D	HVLP2	0.45	Non- Etching	0.43

# III. ANALYSIS AND RESULTS

Figure 5 is Delta-L frequency response of one sample board up to 40GHz. When the post-processing protocol with the physical fitting of advanced root omega is applied to the deembedding raw data, it can make the reported insertion loss numbers in Fig. 5 (b) more error-resistant. Table IV shows Delta-L results in dB per inch with an average value of three testing samples at 4 GHz, 8 GHz, 16 GHz, 25 GHz, and 32 GHz, respectively. In Table V, Sample B is taken as the base line to investigate copper foil change and oxide treatment impact. After oxide alternative treatment in HVLP and HVLP2, the surface roughness of sample A and B are almost the same and the insertion loss are very similar. According to this experiment, the electrical performance cannot be improved significantly by copper foil type change without the proper surface treatment. When the surface treatment changes to low etching (Sample C) and non-etching type (Sample D), the reduction are 8% and 10% at 25 GHz, respectively. HVLP2 with the surface treatment of non-etching is the best one in the loss and the enhancement by non-etching approach is more when the frequency is higher. It implied the oxide treatment is very critical besides the inherent copper type.



(a) De-embedding raw data



(b) Physical fitting Fig. 5. Delta-L result in dB/inch up to 40GHz

Copyright © 2019 IEICE

0.273

D

0.418

Table IV. Delta-L results

Table V. Loss reduction comparison in percentage

0.666

0.916

1.098

Loss Reduction (%)	4GHz (dB/in)	8GHz (dB/in)	16GHz (dB/in)	25GHz (dB/in)	32GHz (dB/in)
А	1%	-1%	-2%	-2%	-2%
В	-	-	-	-	-
С	3%	5%	7%	8%	8%
D	4%	6%	9%	10%	11%

## IV. CONCLUSION

In this study, the choice of copper foil type and oxide surface treatment is affecting insertion loss characteristics to a significant amount. The electrical characteristics of the design by the conventional oxide alternative with a higher etching rate (larger roughness) performed worse, especially when the frequency is going higher. Surface treatment is very critical to the electrical performance when adopted the smoother copper foil of HVLP2 in ultra low-loss PCB design. To achieve better SI performance for higher frequency application, HVLP2 copper foil combine with lower or non-etching surface treatment can reach the lower insertion loss since the profile surrounded the conductor is the smoothest.

# V. ACKNOWLEDGMENT

The authors would like to thank KJ Lu for coordinating overall test preparation, Allied Circuit Co., Ltd. for manufacturing test vehicles, Electromagnetic Compatibility Laboratory of Missouri S&T for 40 GHz testing metrology development, Litek and MPI Corporation for high-frequency measurement supports, MEC Co. and Atotech Co. for provision surface treatment in this study.

#### References

- G. Brist, S. Hall, S. Clouster, T. Liang, "Non-Classical Conductor Losses due to Copper Foil Roughness and Treatment", Electronic Circuits World ConventionProceedings, 2005, vol. 10, p. 22-24
- [2] SeiyaKido, TsuyoshiAmatani, "Influence of Copper Conductor Surface Treatment for High Frequency PCB on Electrical Properties and Reliability"
- [3] Thomas Devahif, "ULTRA LOW PROFILE COPPER FOIL FOR VERY LOW LOSS MATERIAL", Proceedings of SMTA International, Sep. 25 - 29, 2016, Rosemont, IL, USA
- [4] IPC-TM-650, Test Methods to Determine the Amount of Signal Loss on Printed Boards
- [5] J. Hsu, T. Su, K. Xiao, X. Ye, S. Huang, Y. Li, "Delta-L Methodology for Efficient PCB Trace Loss Characterization", Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), 2014 9<sup>th</sup> International (pp. 113-116). IEEE.
- [6] J. Hsu, T. Su, K. Xiao, X. Ye, S. Huang, Y. Li, "Printed Circuit Board Insertion Loss Measurement Metrology Comparison", Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), 2015 10<sup>th</sup> International IEEE.
- [7] Elite 8K refers to EM-890K was the first halgoen free ultra low loss material developed by Elite Material Co., Ltd (EMC). For more information, please visit EMC website at "<u>https://www.emctw.com/zh-TW/products/index</u>"