Modeling and Analysis for MOS Capacitance of TSV Considering Temperature Dependence

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***Abstract*—This paper presents a comprehensive modeling and analysis for the metal-oxide-semiconductor (MOS) capacitance of through silicon via in consideration of the temperature dependence. The MOS effect is physically modeled by a Poisson–Boltzmann equation with the distribution of mobile charge carriers included. Temperature-dependent parameters considered in the analysis are the intrinsic carrier density, permittivity, and bandgap of the silicon. With the equation solved, the variations of MOS capacitance with the bias voltage, operating frequency, oxide charge, and temperature can be obtained. The calculated MOS capacitances under different temperature show a good agreement with the measurement results, which verifies the accuracy of the presented modeling and analysis.**

***Index Terms*—through silicon via, MOS capacitance, temperature dependence, electromagnetic interference**

I. Introduction

Through silicon via (TSV) is a critical structure that enables vertical interconnection between stacks in three-dimensional integrated circuits (3-D IC). Among the resistance-inductance-capacitance-conductance equivalent circuit models for TSVs, the metal-oxide-semiconductor (MOS) capacitance has a considerable impact on the electrical performance of 3-D ICs [1]. On the other hand, temperature-dependent parameters including the carrier densities in silicon can lead to the variation of MOS capacitance, resulting in issues such as electromagnetic interference [2] and signal delay [3]. Considering the aggravated thermal condition and the consequent higher temperature increase in 3-D ICs, it is necessary to carefully model and analyze the MOS capacitance of TSV with the temperature dependence.

For a typical cylindrical TSV, a depletion region is formed in the silicon close to the dielectric-silicon interface when an adequate bias voltage is applied. The maximum depletion radius and corresponding minimum MOS capacitance have been calculated in [3] and [4] by iteration, and the variations of MOS capacitance with the bias voltage and interface charges were later reported [5]–[7]. But the approaches employed are only applicable to the case where the applied ac signal is under a high-frequency operation, since the models are based on the full depletion assumption which neglects the mobile charge carriers (holes and electrons) in the depletion region. With the distribution of carriers included, as in [8] and [9], the characteristics of the MOS capacitance with respect to the bias voltage (*C*–*V*) can be captured for the low-frequency, high-frequency, and deep-depletion operations. But the low-frequency minimum capacitance is treated as the high-frequency one in [8] and [9], where the former is actually larger than the latter [10]. Besides the previous efforts where the modelings are performed at room temperature, the temperature dependence of the MOS capacitance has been considered in [11]–[13]. However, the model in [11] can only capture the maximum depletion width under different temperatures, while the approximations in the calculations in [12] and [13] deviate from the physical reality.

In this paper, a comprehensive modeling and analysis for the MOS capacitance of TSV is performed in consideration of its dependence on temperature. The MOS capacitance is calculated from a physically modeled Poisson–Boltzmann equation with the carrier distribution included. Temperature-dependent parameters including the intrinsic carrier density, permittivity, and bandgap of the silicon are taken into account. Results of the analysis can capture the variations of the MOS capacitance with the bias voltage, operating frequency, oxide charge, and temperature. The accuracy of the presented modeling and analysis is verified by comparing the calculated MOS capacitances under different temperature with those from measurement results in the literature.

II. Modeling for MOS Capacitance of TSV

Different from the planar MOS capacitance which has been extensively studied in the literature [10], [14], the MOS effect of a TSV need to be analyzed in cylindrical coordinates. As shown in Fig. 1, a typical TSV structure is composed of the metal core, the dielectric isolation and the semiconductor substrate. For convenience, the corresponding materials are assumed to be copper (Cu), silicon dioxide (SiO_2) and silicon (Si), respectively.

The total MOS capacitance (C_{mos}) of a TSV is the series combination of the dielectric capacitance (C_{ox}) and the semiconductor depletion-layer capacitance (C_{dep}). While the C_{ox} depends only on the material and geometrical parameters, the

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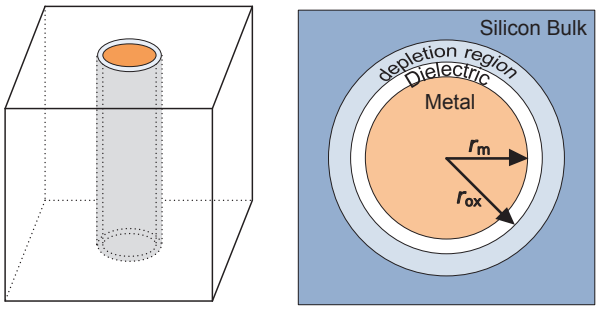

Fig. 1. Geometry of a TSV: (a) 3-D view; (b) top view with the depletion region depicted.

$C_{\rm dep}$ varies with the bias voltage, operating frequency, oxide charge density, and temperature. In the silicon region close to the Si-SiO_2 interface, the distribution of electric charge is assumed to be horizontally axisymmetric and vertically constant, thus the distribution of potential can be described by the following Poisson's equation:

$$\frac{1}{r}\frac{d\varphi}{dr}\left(r\frac{d\varphi}{dr}\right) = -\frac{\rho}{\varepsilon_{\rm Si}} \qquad (r > r_{\rm ox}) \tag{1}$$

where φ and ρ denote the potential and charge density at the radius r, respectively; $r_{\rm m}$ and $r_{\rm ox}$ are the radii of the metal core, and dielectric isolation (SiO_2), respectively; $\varepsilon_{\rm Si}$ is the temperature-dependent permittivity of silicon, which is expressed as follows [15] with the loss tangent ignored:

$$\varepsilon_{\rm Si} = \varepsilon_0 \cdot 11.65 \cdot \left[1 + 1.3 \times 10^{-3} \cdot (T - 293.15)\right] \tag{2}$$

where ε_0 is the vacuum permittivity; T denotes the temperature in Kelvins.

The following analysis is performed for a *p*-tpe silicon substrate, which can be easily converted to the one for a *n*-tpye substrate. According to the carrier distribution in the silicon substrate, the charge density $\rho(r)$ is expressed as

$$\rho(r) = q(-N_A^- + p - n) \tag{3}$$

where q is the elementary charge; N_A^- is the density of the ionized acceptors; n and p are respectively the concentrations of electrons and holes, which are functions of $\varphi(r)$ as shown below, if the applied ac signal varies at a low frequency:

$$n(r) = n_0 \exp\left(\frac{q\varphi}{k_{\rm B}T}\right) \tag{4}$$

$$p(r) = p_0 \exp\left(-\frac{q\varphi}{k_{\rm B}T}\right) \tag{5}$$

where $k_{\rm B}$ is the Boltzmann constant; n_0, p_0 are the equilibrium concentrations of electrons and holes in the bulk of the silicon, respectively. According to the charge neutrality in the bulk of the silicon, far from the surface, the following equation exists:

$$q(-N_A^- + p_0 - n_0) = 0\ . \tag{6}$$

For nondegenerate semiconductors, Boltzmann statistics apply, thus the following mass-action law [10] exists:

$$n_0 p_0 = n_i^2 \tag{7}$$

where n_i is the intrinsic carrier density, which is empirically expressed [11] as

$$n_i = 9.38 \times 10^{19}(T/300)^2 \exp(-6884/T) \quad ({\rm cm}^{-3})\ . \tag{8}$$

For the typical range of operating temperature and doping concentration in 3-D ICs, the silicon substrate is nondegenerate, and almost all dopants are ionized ($N_A^- = N_A$). The Poisson–Boltzmann equation is formulated by substituting the equations from (3) to (8) into (1), which is subsequently solved by using the fourth-order Runge–Kutta method [8], [9] with boundary conditions that the potential (φ) and electric field ($E = -d\varphi/dr$) at the outer edge of the depletion region are equal to zero.

With the obtained potential and electric field in the depletion region, the dielectric capacitance and depletion capacitance per unit height can be expressed as

$$C_{\rm ox} = 2\pi\varepsilon_{\rm ox}/\ln\left(r_{\rm ox}/r_{\rm m}\right) \tag{9}$$

$$\begin{aligned} C_{\rm dep} &= -\frac{dQ_{\rm s}}{d\varphi_{\rm s}} = 2\pi r_{\rm ox}\varepsilon_{\rm Si}\frac{dE_{\rm s}}{d\varphi_{\rm s}} \\ &= 2\pi r_{\rm ox}\varepsilon_{\rm Si}\left[\frac{q}{\varepsilon_{\rm Si}E_{\rm s}}\left(N_A - p + n\right) + \frac{1}{r_{\rm ox}}\right] \end{aligned} \tag{10}$$

where $\varepsilon_{\rm ox}$ is the permittivity of the SiO_2 isolation layer; $Q_{\rm s}$, $\varphi_{\rm s}$, and $E_{\rm s}$ are the charge, potential, and electric field at the surface of the silicon region, respectively. Thus the total MOS capacitance per unit height of the TSV can be obtained as

$$C_{\rm mos} = \frac{C_{\rm ox}C_{\rm dep}}{C_{\rm ox} + C_{\rm dep}}\ . \tag{11}$$

Besides, the bias voltage on the TSV is calculated as [14]

$$V_{\rm G} = V_{\rm FB} + \varphi_{\rm s} - Q_{\rm s}/C_{\rm ox} \tag{12}$$

where $V_{\rm FB}$ is the flat-band voltage, which is expressed as

$$V_{\rm FB} = \phi_{\rm ms} - 2\pi r_{\rm ox}Q_i/C_{\rm ox} \tag{13}$$

where Q_i is the density of the oxide charges in the SiO_2 isolation layer, which can be regarded as a charge sheet located at the Si-SiO_2 interface; $\phi_{\rm ms}$ is the difference of work function between the metal and the silicon, which is calculated as

$$\phi_{\rm ms} = \phi_{\rm m} - \left(\chi + \frac{E_{\rm g}}{2q} + \frac{k_{\rm B}T}{q}\ln(\frac{N_A}{n_i})\right) \tag{14}$$

where $\phi_{\rm m}$ is the work function of the metal; χ and $E_{\rm g}$ are respectively the electron affinity, and the bandgap of the silicon, where the latter is expressed as [10]

$$E_{\rm g} = 1.169 - 4.9 \times 10^{-4}T^2/(T + 655) \quad ({\rm eV})\ . \tag{15}$$

By substituting the equations from (13) to (15) into (12), the bias voltage ($V_{\rm G}$) is obtained as

$$\begin{aligned} V_{\rm G} =& \phi_{\rm m} - \left(\chi + \frac{E_{\rm g}}{2q} + \frac{k_{\rm B}T}{q}\ln(\frac{N_A}{n_i})\right) \\ &- \frac{r_{\rm ox}Q_i}{\varepsilon_{\rm ox}}\ln\left(\frac{r_{\rm ox}}{r_{\rm m}}\right) + \frac{r_{\rm ox}\varepsilon_{\rm Si}E_{\rm s}}{\varepsilon_{\rm ox}}\ln\left(\frac{r_{\rm ox}}{r_{\rm m}}\right) + \varphi_{\rm s}\ . \end{aligned} \tag{16}$$

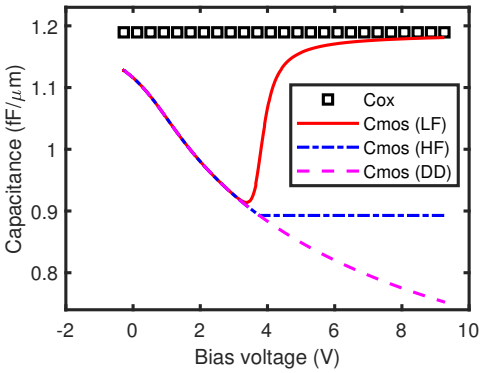

Fig. 2. MOS capacitance of the TSV with respect to the bias voltage under different operations.

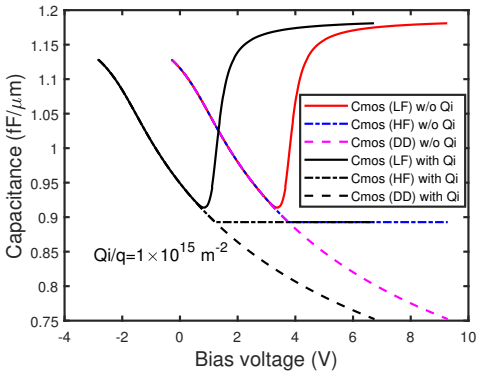

Fig. 3. *C–V* curve of the TSV under different operations with and without oxide charges.

Note that the expression for the density of minority carrier (namely, (4)) is for the low-frequency operating case. In the high-frequency case, the recombination-generation rates of minority carriers can not keep up with the variation of the applied ac small signal. Consequently, the minority carrier density should be rewritten as $n = n_0$. In addition, if the bias voltage is swept at a relatively fast rate so that there is not enough time for the thermal generation of the inversion charge carriers [14], the inversion layer does not form, which is the deep-depletion operating case.

III. Analysis and Verification

The characteristics of the MOS capacitance with respect to the bias voltage (*C–V* curve) vary with the operating frequency, oxide charge density, and temperature, which are respectively discussed in this section.

A. C–V Curve under Different Operating Frequency

By solving the equations in the previous section, the characteristics of the total MOS capacitance with respect to the bias voltage (*C–V*) are captured for the low-frequency (LF), high-frequency (HF), and deep-depletion (DD) operations at room temperature, as depicted in Fig. 2. The applied parameters are: $r_{\rm m}$ = 2.5 μm, $r_{\rm ox}$ = 3 μm. The doping concentration is 2×10^{15} cm^{-3}. The oxide charge density is assumed to be zero here $(Q_i/q = 0)$.

As shown in the figure, the MOS capacitance varies with the applied bias voltage, where the *C–V* curve can be divided into three regimes: accumulation, depletion and inversion. The obtained MOS capacitance $(C_{\rm mos})$ is smaller than the oxidation capacitance $(C_{\rm ox})$, as expected. In addition, the variation of MOS capacitance with the operating frequency are successfully captured, especially in the inversion regime. Under a low-frequency operation, the minority carrier can catch up with the variation of the applied signal, leading to the increase of the MOS capacitance in the inversion regime. Under a high-frequency operation, instead, the MOS capacitance keeps its minimum value after the the bias voltage exceeds the threshold voltage. Under a deep-depletion operation, the inversion layer does not form, thus the MOS capacitance would decrease with the increase of bias voltage.

Note that the minimum MOS capacitance under a high-frequency operation is smaller than the one under a low-frequency operation.

B. C–V Curve with and without Oxide Charge

In this part, the effect of the fixed oxide charges on the *C–V* curve is considered and discussed.

For the oxide charge density with a typical order of magnitude, which is $Q_i/q = 1\times10^{15}$ m^{-2} here, the *C–V* curve is obtained and compared with the one where the oxide charge is ignored. As shown in Fig. 3, there is an obvious shift of the *C–V* curve when the oxide charge is included. This shift can be attributed to the additional gate bias required to achieve the same band bending in the original semiconductor, which is also indicated by (12) and (13).

C. C–V Curve under Different Temperature

In this part, the MOS capacitance under a high-frequency operation is calculated and compared with the measurement results in [11]. The parameters in [11] are: $r_{\rm m} = 2.412$ μm, $r_{\rm ox} = 2.6$ μm. The height of the TSV is 42 μm. The doping concentration (N_A) is 1.45×10^{15} cm^{-3}. The oxide charge density is $Q_i/q = 6\times10^{11}$ cm^{-2}.

In the accumulation regime, the MOS capacitance approximates to the oxidation capacitance and does not vary with temperature. In the depletion and inversion regimes, the high-frequency MOS capacitances under different temperature are calculated, and depicted in Fig. 4. As temperature increases, the *C–V* curve is elevated and shifted. The main reason is that the intrinsic carrier density increases dramatically with the rise of temperature, leading to the reduction of depletion width and the increase of coresponding MOS capacitance. To be specific, the minimum MOS capacitances obtained in this work are compared with those from measurement and model in [11] under different temperatures, as shown in Table I. The calculated results in this work match well with the measured ones in [11], as shown by the listed relative error between them. It also can be observed that the presented model in this

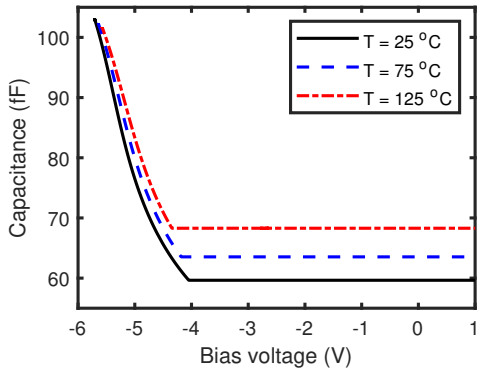

Fig. 4. High-frequency MOS capacitance with respect to the bias voltage under different temperatures.

TABLE I
COMPARISON OF MOS CAPACITANCE BETWEEN MODEL AND MEASUREMENT UNDER DIFFERENT TEMPERATURE

Temperature [°C]	**Results in [11]** [fF]			**This work** [fF]	
	Measured	***Model***	***Err*** [%]	***Model***	***Err*** [%]
25	60.009	60.499	0.81	59.621	-0.65
50	60.303	61.698	2.31	61.496	1.98
75	61.210	62.961	2.86	63.532	3.79
100	63.774	65.187	2.21	65.763	3.12
125	69.229	67.12	-3.04	68.289	-1.36

work is mostly more accurate than the model in [11] which can only capture the minimum MOS capacitance instead of the *C*–*V* curve.

IV. CONCLUSION

A comprehensive modeling and analysis for the MOS capacitance of TSV is performed in this paper. Based on a physically modeled Poisson–Boltzmann equation, the variations of the MOS capacitance with the bias voltage, operating frequency, oxide charge, and temperature are captured. The calculated MOS capacitances under different temperatures are compared with the measurement results in the literature, which demonstrates that the presented modeling and analysis can accurately obtain the MOS capacitance of a TSV and its temperature dependence.

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