Modified Channel Quality Comparison for PCI Express* 4.0

Thonas Su, Denis Chen, Jimmy Hsu, and Y. L. Li

Data Center Platform Application Engineer

Intel Microelectronics Asia LLC, Taiwan Branch

20F, #369, Sec. 7, Zhong-Xiao E. Rd., Nan-Gang District 11561, Taipei, Taiwan (R.O.C.)

Thonas.Su@intel.com, Denis.Chen@intel.com, Jimmy.Hsu@intel.com, Y.L.Li@intel.com

Abstract—**The Channel Quality Comparison (CQC) method was introduced in 2011** [1]**. It is commonly used in the pre-layout simulation to estimate the risk of the channel, for high speed SERDES (Serializer/Deserializer) and DDR interfaces. However, once the equalizer inside the transmitter (Tx) and the receiver (Rx) becomes more and more powerful, the eye height (EH) and the eye-width (EW) will have less difference in thee effective range. Since CQC is a comparative method which relies on comparing the EH and EW between the current channel and the reference one, this phenomenon will introduce uncertainty. Although using the "DOE/RSM" (Design of Experiment /Response Surface Methodology) method may overcome the issue, it simply requires more resource. Not all projects or channels have the luxury to conduct a comprehensive simulation. In this paper, a modified CQC method is proposed to find a balance between speed and the accuracy.**

Keywords—*Channel Quality Comparison; CQC; DOE; UPM;*

I. INTRODUCTION

Conduct the channel simulation is the best way to understand the risk before having a real system. Since most of the electronic devices have components on PCB board(s), two terms, "pre-layout simulation" and "post-layout simulation", are commonly used to distinguish the timeframe, the target, as well as the procedure in the early design phase and the PCB layout phase, respectively.

- Pre-layout simulation

  In the early design phase, the purpose of conducting simulation is to find the solution space (or, at least, a solution point) or search the possibilities among different routings and connection strategies. I/O models like the spice mode, the behavior model, or the IBIS-AMI model may be used in each side of the channel. The transmission line, the via, the connector, the cable, and he package model are used to form the channel. Through the simulation, receiver waveform will be obtained and an eye diagram will be calculated to understand the channel's electrical performance. For Intel server group's customers, either CQC or DOE/RSM/UPM method is suggested to conduct the pre-layout simulation.

- Post-layout simulation

  Once the simulation engineer comes out a conclusion from the pre-layout simulation, rules (e.g. length, trace-to-trace spacing, routing layer, via stub, etc.) will be provided to the layout engineer. When the project is close to tape-out, the hardware and the layout engineer will conduct layout check to avoid rules' violations. In the meantime, the simulation engineer may help to check the channel's layout by conducting simulation. For example, the Intel server group has the "CCT layout check procedure" which is not based on "rules" but on "electrical performance".

To minimize the time and effort for Intel's customers, Intel's internal simulation team will conduct the pre-layout simulation based on assumptions (e.g. board size, component placement, cable and PCB material). A platform design guide (PDG) will be released to customers. Customers' projects which reside within the PDG's solution space (a.k.a. PDG compliance) do not require to conduct simulation. However, different designs have different topologies and limitations. Many projects which cannot follow the PDG will require to conduct simulation to understand the risk of the channel.

II. CHANNEL QUALITY COMPARISON

Although DOE/RSM method is commonly used in the industry, it requires to conduct simulation based on a large case number (e.g. 128 cases or more for one scenario). Sometimes it will be the bottleneck because not all Intel customers have multiple Electronic Design Automation (EDA) tool licenses to simulate the channel response and calculate the eye diagram (EH and EW). Moreover, the simulation engineer may only has several days to conduct the analysis, instead of weeks or months. In 2011, the Channel Quality Comparison (CQC) method was introduced to Intel server group's customers to address this difficulty. The CQC is a comparative method by comparing the eye diagram of the current channel to a reference one.

- Reference Channel

  The reference channel is usually a topology inside the Platform Design Guide (PDG). Since Intel server group releases the I/O models, channel libraries, and some example channels to Intel's customers, the eye diagram can be simulated and acted like a reference.

---

* Other names and brands may be claimed as the property of others.

- Current Channel

    If the current channel has a larger eye diagram from the simulation result, it implies the risk is low. On the contrary, the smaller of the EH/EW, comparing with the reference, the higher risk this channel might be.

To have an apple-to-apple comparison, a typical corner assumption (e.g. normal impedance, normal termination value, etc.) is used on the current channel and the reference one.

In the old days, the transmitter (Tx) may only have 1 tap of equalization (eq.) and receiver (Rx) may not have any. Starting from PCI Express* (a.k.a. PCIe*) 3.0, both Tx and Rx have equalization and the latest PCIe* 4.0 have better Rx equalization than its predecessor. Because these equalization mechanisms will try their best to increase the eye diagram, it is not easy to have a clear difference in the eye diagram, as shown in the Fig. 1.

A stripline open-field length sweeping from 10 to 18 inch in a M.2 PCIe* 4.0 channel is conducted in the simulation. Two different PCB materials, middle loss (ML) and low loss (LL), are considered. The eye height margin (EHm, EHm = EH - min. EH requirement) and eye width margin (EWm, EWm = EW - min. EW requirement) are shown in different colors. The trend (moving average) of EHm and EWm are also plotted.
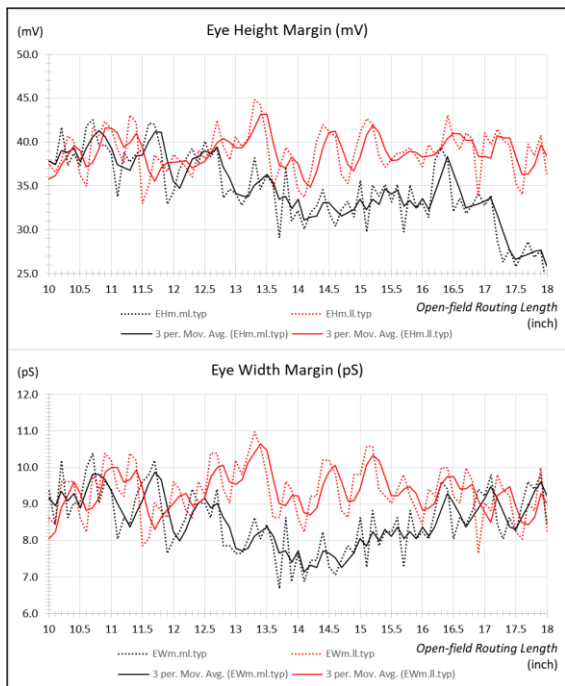

Fig. 1.   Eye Height Margin (mV) and Eye Width Margin (pS) by Using the CQC Method

In this experiment, although the Tx eq. has been locked into a fixed value, the CTLE (Continuous Time Linear Equalizer) and the DFE (decision feedback equalizer) in the Rx are both functioning well in a wide range. Therefore, it is not easy to compare the EH/EW margin values to find the solution space between these 2 PCB materials, ML and LL.

It is possible to use different indicators for comparison [2],[3] or using a different method [4]. For example, the channel

performance by using Pseudo-eye is shown in the Fig. 2. From the channel designer's point of view, this result is more straightforward and can provide an estimation in how much length extension by using LL PCB material. For example, if the PDG suggests to have an 11.5 inch (open-field routing length) with ML PCB material, the LL PCB material might extend the length to 16.0 inch (estimated).
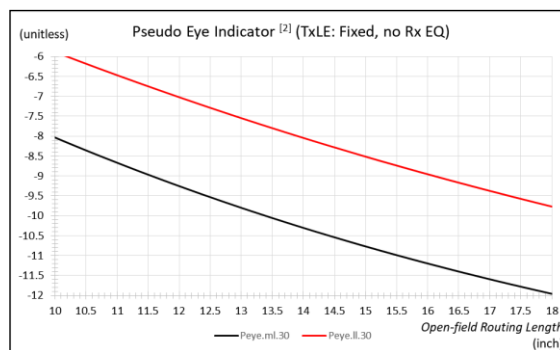

Fig. 2.   Pseudo_eye Indicator by Using the CQC Method

Although using the Pseudo-eye indicator [2] may provide insights, some Intel's customers still prefer to use the eye diagram under a curtained BER (Bit Error Rate). Another possibility is to turn off the equalization in the simulator. It should have a similar result as the Pseudo-eye indicator. However, a negative EHm and EWm will usually be observed in this scenario. Sometimes the value will be saturated in a negative value and will make a comparison more difficult. Moreover, turning off Tx and/or Rx eq. will obstruct the chance to study the equalization effect on compensating the channel loss and discontinuities.

III.   MODIFIED CHANNEL QUALITY COMPARISON

In the original CQC method, a "typical corner" assumption is selected during simulation. Using a typical corner is a very convenient and straightforward approach but will encounter the issue described in the previous section.

Since Intel's internal simulation teams have conducted detailed simulation on each topology, which is documented in the corresponding PDG as well as in the corresponding simulation decks, it is possible to understand the channel behavior under different corners.

A "worse corner" (not need to be the "worst corner") is proposed and suggested to be used in the "Modified CQC Method". A worse/worst corner can be predicted by using a commercial statistical tool, as shown in the Fig. 3. It is not necessary to find the "worst" corner all the time.

In the Fig. 4, a worse corner is selected and a same open-field length sweeping simulation is conducted by using these 2 PCB materials. Similar as the CQC, a potential solution space can be quickly predicted by using the reference channel's result. For example, the PDG may only have a ML PCB material for this topology. If Intel's customers want to use LL PCB material to have a longer routing, using the ML result on the PDG boundary is feasible. In this case, 11.5 inch under ML is selected and a potential solution for LL PCB material is around 16.5 ~ 17.0 inch.
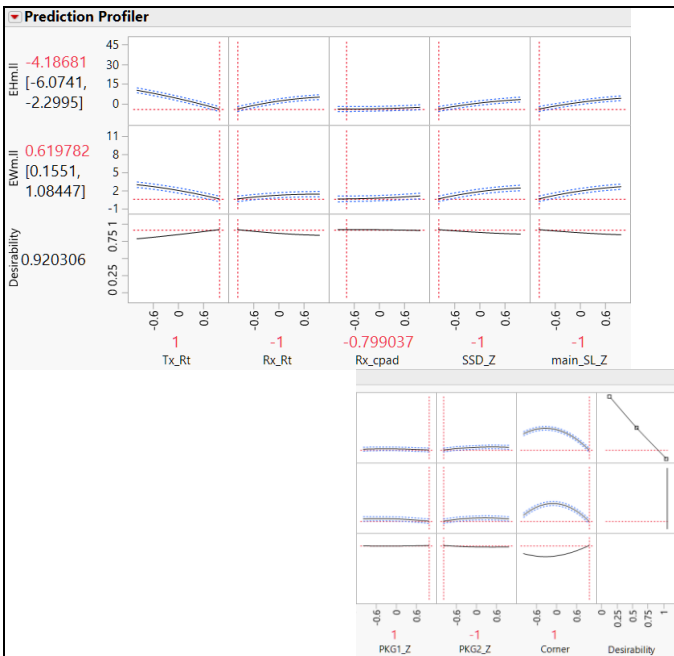
Fig. 3.   A Worst Coner Predicton Based on Min. Eye Height Margin (mV)
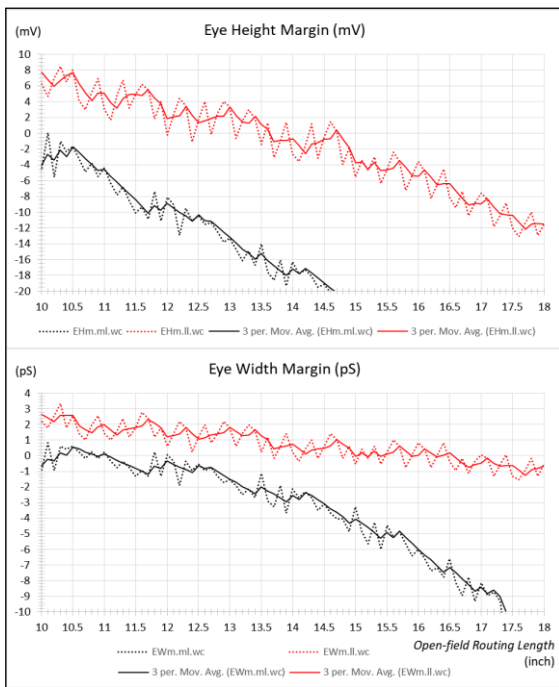

Fig. 4.   Eye Height Margin (mV) and Eye Width Margin (pS) by Using the Modified CQC Method

If the time is limited, using a conservative value, 16.5 inch in this case, is suggested. If the project requires to have a more comprehensive simulation, a DOE/RSM/UPM (Design of Experiment/Response Surface Methodology/Units per Million) method may be used to either validate the solution space coming from the "Modified CQC Method" or to understand the "sensitivity" of these channel variables, especially the channel is close to the design boundary.

By comparing the Fig. 2 with Fig. 4, it explains a reason why some Intel's customers prefer to use the EH/EW result. Although the Pseudo-eye indicator is nice, the design target for PCI Express* is still based on EH and EW in the time domain. A small uncertainty can be accepted if the solution space is enough. However, some customers who want to push their channel designs to the limit may want to reduce this additional margin introduced by using different indicators.

IV. WORSE/WORST CASE

In the Modified CQC Method, a worse/worst corner assumption is used. Using the commercial statistical tool can provide the prediction of it. For these topologies which have the DOE/RSM results, Intel's customers can use them to predict the worse/worst corner. Sometimes, a worst case may have a parameter value which is not on the boundary. For example, an impedance variation is usually represented as [min, typ, max] = [-1, 0, 1]. The worst case may be located at "-0.967" for this variable. In this case, "-1" can still be used unless there is a huge EH/EW difference between "-0.967" and "-1". A prediction of the "worst corner" on EH (eye height) conducted by a commercial statistical tool is shown in the Fig. 3. These values in this corner may be used in the Modified CQC Method. Please notes that different topologies will have different worst corners.

Once a different indicator is used (e.g. change from EH/EW to Pseudo-eye), the "Prediction Profiler" may be changed. This is the major reason some Intel's customers prefer using EH/EW directly because they want to understand the effects of these variables to further optimize the channel or to reduce the cost based on the eye diagram, instead of other indicators.

V. FLOWCHART

The "Modified Channel Quality Comparison (CQC) Method" simulation flowchart is shown in the left side of the Fig. 5. The designer first may get a worse/worst corner from the DOE/RSM simulation result from a reference channel (a1). After then, use this corner assumption and conduct a length sweeping is required (a2).
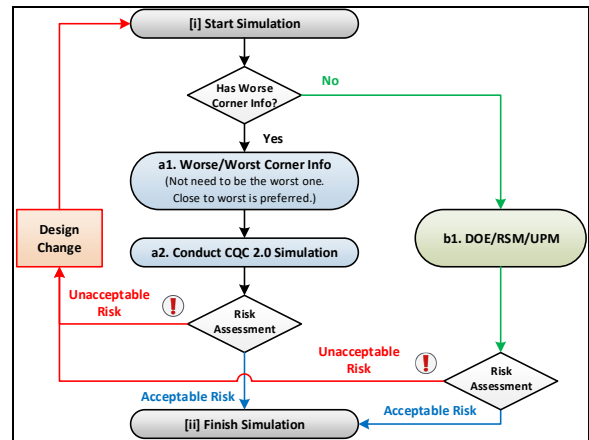

Fig. 5.   Flowchart of the Modified Channel Quality Comparison Method

The minimum length sweeping length is usually a 0.5 inch distance with a 0.1 inch step size for a SERDES interface like

PCIe* 3.0 and 4.0. In summary, at least 6 cases from the target design and 6 cases from the reference design will be simulated and compared. The reference channel usually comes from the Intel server platform's PDG but should not be limited. It may come from other existing project which had been either well simulated or validated. In the "Modified CQC", selecting a reference channel which is close to the design topology is still preferred. If the resource is allowed, a wider length sweeping range can provide a better picture of the channel's performance.

In this example, using the ML and LL PCB material will have a larger insertion loss difference because of the long open-field routing length. Since the reference channel use ML PCB material, either the designer needs to estimate a potential landing zone in advance or use a wider length sweeping range. This is the reason a range from 10 to 18 inch is selected and compared in the previous section, as shown in the Fig. 4.

VI. Verification

The worse EH/EW under different open-field routing length have been provided and shown in the Fig. 4. Sometimes the worse/worst case's eye diagram is too pessimistic and the eye height margin (EHm) as well as the eye width margin (EWm) will be below the requirement (smaller than 0). To proof the final UPM (Units per Million, a.k.a. DPM) is still acceptable (Requirement: UPM < 50), the UPM results by using ML and LL PCB materials are provided in the Table I.

TABLE I.   The UPM Result By Using Different PCB Materials

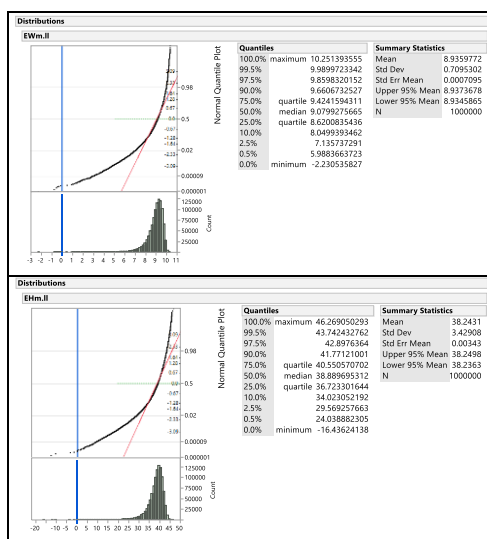| PCB Material	Open-field Length (inch)	UPM (number)	Notes
Middle Loss (ML)	11.5 inch	EH: 11 EW: 12	Reference channel in the Platform Design Guide (PDG)
Low Loss (LL)	15.5 inch	EH: 2 EW: 1	
	16.5 inch	EH: 5 EW: 6	
	17.5 inch	EH: 58 EW: 11	Not acceptable (UPM>50)

Fig. 6.   UPM Result of EHm and EWm (16.5" Open-field Routing, LL PCB)

From the "Modified CQC", a possible solution boundary is located around 16.5 ~ 17.0 inch (the open-field length) when LL PCB material is used. In this example, DOE/RSM/UPM values for 15.5, 16.5, and 17.5 inch are calculated to understand the risk. It is obvious that 17.5 inch may not be acceptable because the EH's UPM is larger than 50. The 16.5 inch is acceptable because the EH's and EW's UPM values are 5 and 6, receptively. The EHm and EWm distributions are shown in the Fig. 6.

VII. Summary

In the server industry, different designs have different usages, mechanical limitations, and operation environments. There are many high-speed SERDES and DDR channels inside the system. Some of these channels might be more challenging than the others due to the connection strategy, the routing complexity, and the cost limitation. Having different simulation methods is very important because a high risk channel may require a comprehensive simulation but a low risk one may only need a quick check.

In this paper, an improved method, the "Modified CQC", is introduced. Use the worse/worst corner assumption can overcome the issue introduced by these Tx and Rx equalization mechanisms when using the original CQC. This can only be achieved by leveraging the simulation result from the Intel's internal simulation team. Intel's customers can estimate the risk of their channel without conducting a full DOE/RSM/UPM simulation when the information required by the "Modified CQC Method" is available. This provide a better flexibility for signal integrity engineers to complete the simulation within a limited time as well as reduce the TTM (time to market) for Intel's customers.

References

[1] Y. Li, X. Ye, K. Xiao, T. Su, K. Kang, "Channel Quality Comparison for OOG IO Bus Designs," in Proc. Intl. Conference on Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), pp. 761-763, 2011.

[2] Y. Li, K. Xiao, X. Ye, Y. Zhu, E. Hsiung, T. Su, K. Wu, J. Hsu, and K. Kang, "Board-level signal integrity methodology," in Proc. Intl. Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), pp. 217-219, 2012.

[3] J. Hsu, T. Su, Y. Li, E. Hsiung, K. Xiao, X. Ye, K. Wu, "Fast Signal Integrity Methodology for PCB Pre-layout Analysis and Layout Quality Check," in Proc. Electronic Components and Technology Conference (ECTC), pp. 2012-2017, 2013.

[4] D. Chen, T. Su, J. Hsu, Y. Li, "Advanced Channel Analysis Method using Channel Quality Comparison and Design of Experiments," in Proc. Intl. Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), 2018.