# Modeling and Analysis of Multiple Coupled Through-Silicon Vias (TSVs) for 2.5-D/3-D ICs

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***Abstract*—In this paper, we, for the first time, modeled and analyzed through-silicon vias (TSVs) in the multi-conductor transmission. TSV is one of the essential technology for 2.5-D/3-D ICs. Definitely, a significant number of TSV must be integrated for the direct vertical interconnections. In this point of view, it is important to propose the accurate modeling and analysis for the multiple coupled-TSVs. Firstly, we utilized the loop inductance matrix to model the self- and mutual-inductance respectively. With the assumption of the quasi-TEM propagation, the capacitance and conductance matrix were subsequently calculated to model the self- and mutual- components. The proposed multi-conductor TSVs model was compared with an electromagnetic (EM) solver. The analysis of TSVs was performed based on the insertion loss at frequencies ranging from 0.01 GHz to 20 GHz. From the proposed modeling methodology, the evaluation of an electrical performance for the multiple numbers of TSVs becomes possible. In addition, signal coupling paths were discussed based on the proposed equivalent circuit model and it was observed that the equivalent conductance path is dominant in the signal couplings.**

***Keywords—Through-silicon via (TSV), Multi-conductor transmission, Insertion loss, Silicon interposer***

## I. INTRODUCTION

High bandwidth and density memory interface are absolutely required to achieve superior system performance. Through-silicon via (TSV) technology have been drawn a lot of attentions because it is the key to make 2.5-D/3-D ICs due to its ability to realize the direct vertical interconnections. In addition, it can contribute to implementing a low power and latency system compared to the conventional wire-bonding system. High bandwidth memory (HBM) in particular has adopted a wide input/output (I/O) scheme with a lot of TSVs [1]. Recently, the number of a stacked memory die for HBM is reaching to 8 with more than 30,000 TSVs. For the physical layer (PHY) of HBM, a silicon interposer must be designed because of the wide I/O architecture of HBM. Therefore, a significant number of TSVs must be also integrated in a silicon interposer for the interconnection to the package substrate.

The conceptual view of a silicon interposer with HBM and graphic processing unit (GPU) is illustrated in Fig.1. In the middle of HBM, TSVs are designed to transmit the signal and power from the bottom to the top. Also, in a silicon substrate, TSVs are designed for the stable power supply as well as the signals for GPU and HBM from the package substrate. In this point of view, it is important to characterize the electrical performance of the multiple coupled TSVs. Without the consideration of the effects from adjacent TSVs, the electrical performance of system cannot be precisely evaluated. Several papers have investigated the electrical performance in the coupled TSVs. However, the partial inductance based modeling approach is difficult to apply for multiple coupled TSVs. Moreover, the modeling of the capacitance and conductance components among the TSVs is very complex [2]. The modeling method using the coupling coefficient may occur errors and it is hard to generally apply to different types of TSV designs [3].

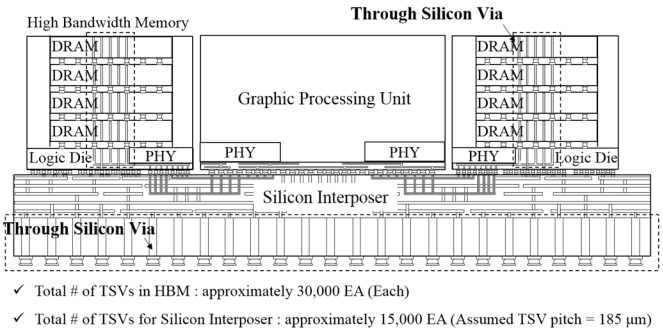


Fig. 1. The conceptual view of a silicon interposer with HBMs and GPU. High bandwidth and density system can be achieved based on the ultra-fine pitch interface. Thousands of TSVs are designed for HBM and a silicon interposer.

In this paper, the simple modeling methodology for multiple coupled TSVs is proposed. In the proposed method, the loop inductance matrix is utilized to simultaneously modeling all inductance components among the TSVs in the condition of a uniform current density. Then, based on the inductance matrix, all capacitance and conductance components valid at the multi-conductor transmission line (MTL) can be simply obtained. For the verification, the proposed equivalent circuit model of TSVs was compared with the electromagnetic (EM) solver from ANSYS. The analysis of insertion loss was conducted at the frequencies ranging from 0.01 GHz to 20 GHz. From the equivalent circuit models, it is possible to analyze the coupling paths between the TSVs.

## II. THE PROPOSAL OF MODELING MULTIPLE COUPLED-TSVS BASED ON THE MULTI-CONDUCTOR TRANSMISSION

In this section, the modeling methodology for multiple coupled TSVs is proposed with the various design parameters.

The resistance, inductance, capacitance, and conductance of TSVs were modeled to build the equivalent circuit model.

### *A. Physical dimension and material properties of TSVs*

The design parameters and material properties used in this paper are depicted and summarized in Fig. 2 and Table I respectively. Considering the typical aspect ratio of TSV and material properties of a semiconductor process, design and analysis of multiple coupled TSVs were conducted. But the proposed equivalent circuit model is scalable, the values in the table are used for the verification with the EM simulation.

### *B. RLGC modeling of multiple coupled TSVs*

Firstly, the equivalent resistance of TSV is driven from the solution of Bessel-function (1) [4]. In this paper, the internal inductance of TSVs which can be obtained from the imaginary term of the solution is ignored.

$$R_{TSV} = Real\left(\frac{(1-j)J_0((1-j)(d_{TSV}/2)/\delta_{cu})}{\sigma_{cu}(2\pi(d_{TSV}/2)\delta_{cu}J_1((1-j)(d_{TSV}/2)/\delta_{cu})}\right)/2 \quad (1)$$

The self- ($L_{i,i}$) and mutual inductance ($L_{i,j}$) terms are calculated using (2-3). Where, $p_{TSVi0}$ stands for the pitch between the $TSV_i$ and reference $TSV_1$ [5].

$$L_{i,i} = \frac{\mu h_{TSV}}{\pi} ln\left(\frac{p_{TSV_{i0}}}{d_{TSV}/2}\right) \quad (2)$$

$$L_{i,j} = \frac{\mu h_{TSV}}{2\pi} ln\left(\frac{p_{TSV_{i0}} p_{TSV_{j0}}}{P_{TSV_{ij}}(d_{TSV}/2)}\right) \quad (3)$$

Based on the loop inductance matrix, the capacitance matrix can be calculated with the relationship in (4) [6].

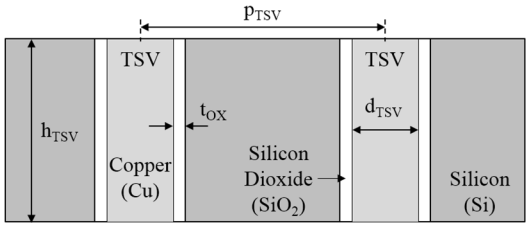


Fig. 2. Design parameters of TSVs are depicted. The pitch, diameter, height, and the thickness of insulator of TSVs are the main parameters discussed in this paper.

TABLE I. THE PHYSICAL DIMENSION AND MATERIAL PROPERTIES OF THE PARAMETERS FOR TSVS

| Parameter | *Symbol* | *Value* |
|---|---|---|
| The diameter of TSV | $d_{TSV}$ | 10 μm |
| The height of TSV | $h_{TSV}$ | 100 μm |
| The pitch of TSV | $p_{TSV}$ | 200 μm |
| The thickness of $SiO_2$ | $t_{ox}$ | 0.5 μm |
| The relative permittivity of Si | $\varepsilon_{Si}$ | 11.9 |
| The relative permittivity of $SiO_2$ | $\varepsilon_{SiO2}$ | 4.1 |
| The conductivity of Si | $\sigma_{Si}$ | 10 S/m |
| The conductivity of Cu | $\sigma_{Cu}$ | $5.8\times10^7$ S/m |

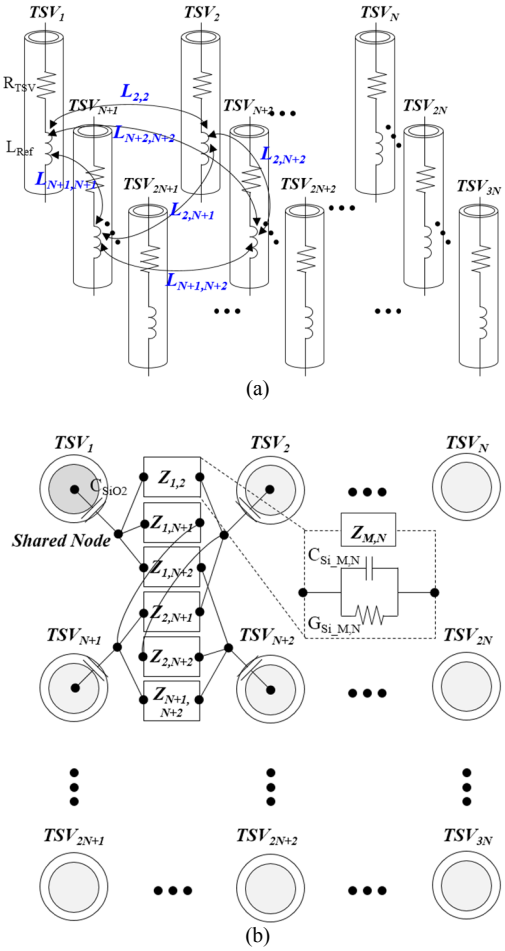


Fig. 3. The equivalent circuit model of proposed TSV model. (a) The resistance and inductance are depicted. (b) The capacitance and conductance are depicted. For the intuitive understanding, the circuits are represented in case of the 2-by-2 TSVs.

$$\begin{bmatrix} C_{1,1}+\cdots+C_{1,3N} & -C_{1,2} & \cdots & -C_{1,3N} \\ -C_{12} & C_{2,1}+\cdots+C_{2,3N} & \cdots & -C_{2,3N} \\ \vdots & \vdots & \ddots & \vdots \\ -C_{3N,1} & -C_{3N,2} & \cdots & C_{3,1}+\cdots+C_{3,3N} \end{bmatrix} = \mu_0\varepsilon_0\varepsilon_{si}h_{TSV}{}^2 \begin{bmatrix} L_{1,1} & L_{1,2} & \cdots & L_{1,3N} \\ L_{1,2} & L_{2,2} & \cdots & L_{2,3N} \\ \vdots & \vdots & \ddots & \vdots \\ L_{3N,1} & L_{3N,2} & \cdots & L_{3N,3N} \end{bmatrix}^{-1} \quad (4)$$

When modeling above loop inductance matrix, the term ($d_{TSV}/2$) must be substituted with the term ($d_{TSV}/2 + t_{ox}$) to include the dielectric thickness. Then, the conductance matrix can be obtained by (5).

$$C_{M,N} = C_{Si\_M,N} = \frac{\sigma_{Si}}{\varepsilon_0\varepsilon_{Si}} G_{Si\_M,N} \quad (5)$$

Lastly, the capacitance of the silicon dioxide insulator around TSV is expressed as (6).

$$C_{SiO2} = \frac{2\pi\varepsilon_0\varepsilon_{SiO2}}{ln(d_{TSV}/2 + t_{ox})/(d_{TSV}/2)} \quad (6)$$

## III. The Analysis of Multiple Coupled TSVs and The Verification with EM Simulations

In this section, the analysis of multiple coupled TSVs based on the proposed equivalent circuit model and EM simulation was conducted. From the insertion loss, the proposed model for the TSVs can be successfully verified. In addition, the dominant parameters affecting to the electrical performance of TSVs are also evaluated depending on the frequency range. Lastly, the signal coupling paths between the TSVs are discussed to propose the direction to efficiently reduce signal couplings.

### *A. The analysis of insertion loss for multiple coupled TSVs*

Total 5 cases considering the number and location of ground TSV were designed to analyze in the various conditions as depicted in Fig. 4. The TSV located in the center of TSV array named victim is analyzed as a target channel. The insertion loss based on the proposed model and EM simulation for different cases are plotted in Fig. 5 at the frequencies ranging from 0.01 MHz to 20 GHz. The proposed model shows an absolutely good agreement compared with the EM simulation regardless of the cases. In the figure, the equivalent term (Eq) means that the effective value of a single TSV. For example, the equivalent capacitance ($C_{Eq}$) includes the self- and mutual- capacitance.

From the equivalent circuit model, it can be observed that the equivalent resistance which is related to the dc/ac conductor loss mainly affects the electrical characteristics under the 300 MHz frequency range. In the high frequency above the 300 MHz, the equivalent capacitance and conductance becomes dominant so that the insertion loss is rapidly increased. Especially, above the 2 GHz frequency range, the effects of conductance becomes stronger than those of capacitance. The insertion loss varies depending on the equivalent conductance. When the equivalent conductance of TSVs becomes smaller, the insertion loss is increased due to the high impedance. Therefore, above the 5 GHz, the difference of the TSV conductance mainly makes the different electrical characteristics of TSVs.

The insertion loss of multiple coupled TSVs with 3 ground which is not discussed in the paper is also conducted. But the insertion loss is not much improved compared to 2 ground TSV cases. Because the insertion loss becomes saturated regardless of the numbers of ground TSVs, it is important to evaluate the signal couplings together. When determining the number of ground TSVs, it must be performed to determine to find out the saturation point to prevent over ground design. But the impact of signal couplings from the adjacent TSVs must be also proceeded for the signal integrity optimization.

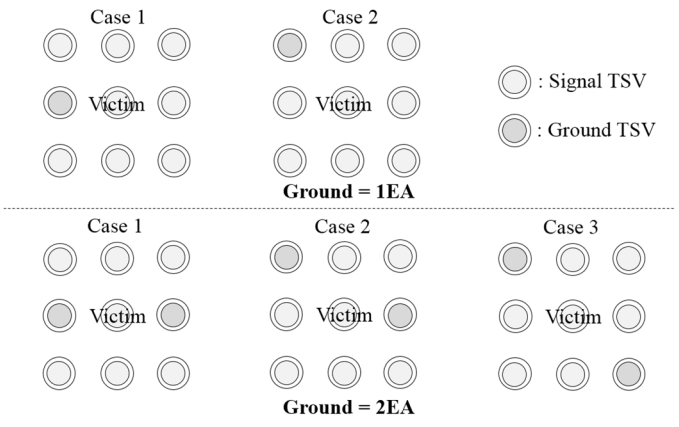


Fig. 4. Various coupled TSV designs for the modeling verification with the analysis. The target TSV (Victim) to be analyzed is located in the center of TSV array.

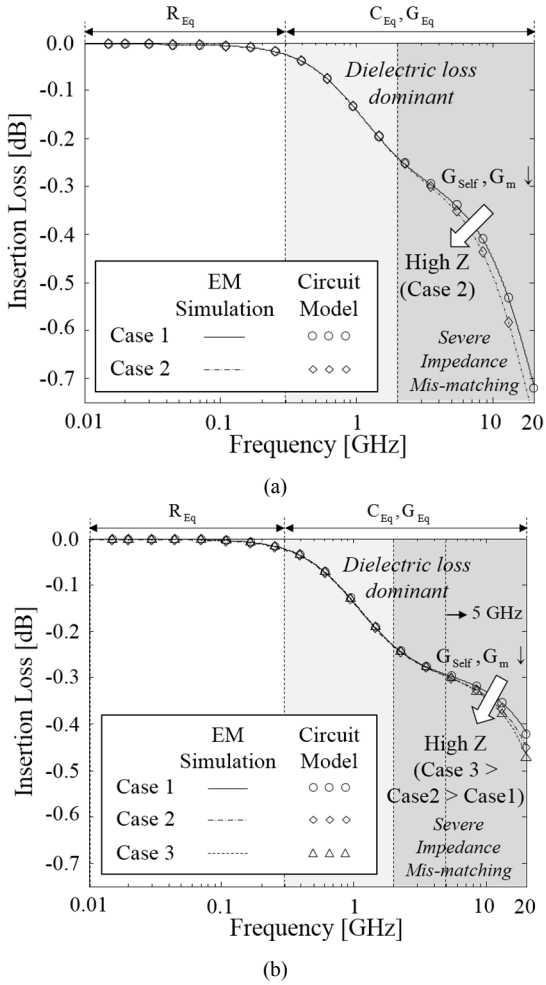


Fig. 5. Insertion loss of multiple coupled TSVs in different cases from the proposed equivalent circuit model and EM simulation. (a) In 1 ground TSV designs, insertion loss is severely degraded due to the impedance mis-matching. (b) In 2 ground TSV designs, insertion loss is slightly degraded depending on the value of self and mutual conductance.

### *B. The analysis of signal coupling paths between TSVs*

From the proposed equivalent circuit model, it is verified that the model can be applied for the evaluation of signal characteristics. The analysis of signal couplings was also conducted in the time domain between the signal TSVs. The simple equivalent circuit model is depicted in Fig. 6. There are mainly two signal paths existed. One is the path related to the conductance of a silicon substrate. The other is the path related to the capacitance of a silicon substrate. Including the capacitance ($C_{SiO2}$) from the silicon dioxide around TSVs, the total equivalent conductance and capacitance between the signal TSVs can be written as (7)-(8).

$$C_{Eq} = \frac{2C_{TSV}(G_{Si}^2+C_{Si}\omega^2(C_{Si}+2C_{TSV}))}{G_{Si}^2+\omega^2(C_{Si}+2C_{TSV})^2} \quad (7)$$

$$G_{Eq} = \frac{4G_{Si}C_{TSV}^2\omega^2}{G_{Si}^2+\omega^2(C_{Si}+2C_{TSV})^2} \quad (8)$$

From the equivalent capacitance ($C_{Eq}$) and conductance ($G_{Eq}$), it is possible to predict the dominant factor. The equation (7)-(8) can be approximated into (9)-(10) in the high frequency range.

$$C_{Eq} = \frac{2C_{TSV}(C_{Si}\omega^2)}{\omega^2(C_{Si}+2C_{TSV})} \quad (9)$$

$$G_{Eq} = \frac{4G_{Si}C_{TSV}^2\omega^2}{\omega^2(C_{Si}+2C_{TSV})^2} \quad (10)$$

The conductance of a silicon substrate ($G_{Si}$) is dominant and the capacitance of a silicon substrate ($C_{Si}$) is ignorable at the high frequency range. It can be easily predicted that the path 1 is the main signal path for couplings, because the conductance term ($G_{Si}$) due to a silicon substrate is in the equation (8).

The time domain simulations to support the analysis were conducted as plotted in Fig. 7. The coefficients (A and B) are intentionally added to evaluate which signal path is critical. Even if the coefficient B is varied, the magnitude of coupled signals is not dynamically changed. However, the magnitude of coupled voltage becomes twice when the coefficient A is set to 5. From the equations and time domain simulations, it is recommended to design the low conductance of a silicon substrate to reduce signal couplings.

## IV. Conclusion

For 2.5-D/3-D ICs, TSV technology must be applied to improve the system performance. A significant number of TSVs are integrated for the vertical interconnection. In this point of view, the modeling and analysis of multiple coupled TSVs must be conducted to characterize the electrical performance. Based on the assumption of a uniform current density in TSVs, we successfully propose the modeling methodology to consider self- and mutual components among the TSVs. To improve the accuracy of the model, the solution of Bessel-function and the loop inductance matrix are used. The proposed modeling shows a good agreement with EM simulations.

The insertion loss of multiple coupled TSVs depending on the numbers of ground and the location of ground is analyzed at the frequencies ranging from 0.01 GHz to 20 GHz. The results show that the equivalent conductance of TSVs mainly determines the insertion loss which is dominantly affecting to the impedance. In addition, from the time domain simulation, it is observed that the conductance of TSVs is the key factor of signal couplings.

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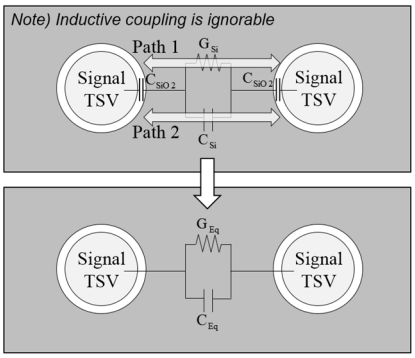


Fig. 6. The circuit model between the signal TSVs. The path 1 where the signals are coupled due to the conductance of a silicon substrate and the path 2 where the signals are coupled from the capacitance of a silicon substrate are indicated. The equivalent conductance and capacitance are calculated for the analysis.

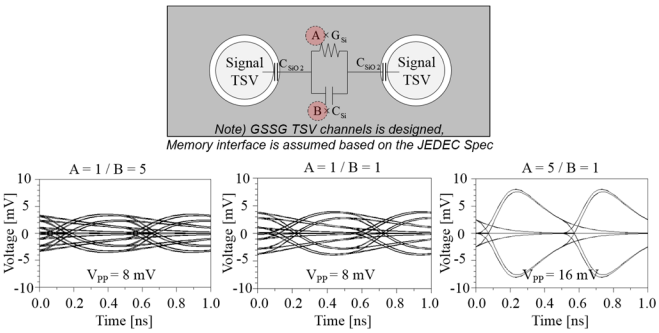


Fig. 7. The magnitude of coupled voltage depending on the conductance and capacitance. To find out the dominant factor, the coefficients (A and B) are intentionally taken into account in the circuit simulation. It is obvious that the conductance of a silicon substrate plays an important role as a signal coupling path.

## References

[1] Standard, J. E. D. E. C. (2015). HIGH BANDWIDTH MEMORY (HBM) DRAM. JESD235A.

[2] J. S. *Pak* et al., "PDN Impedance Modeling and Analysis of 3D TSV IC by Using Proposed P/G TSV Array Model Based on Separated P/G TSV and Chip-PDN Models," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 1, no. 2, pp. 208-219, Feb. 2011.

[3] K. Salah, H. Ragai, Y. Ismail and A. E. Rouby, "Equivalent lumped element models for various n-port Through Silicon Vias networks," *16th Asia and South Pacific Design Automation Conference (ASP-DAC 2011)*, Yokohama, 2011, pp. 176-18

[4] S. A. Schelkunoff, "The electromagnetic theory of coaxial transmission lines and cylindrical shields," Bell Syst. Tech. J., vol. 13, no. 4, pp.532-579, 1934.

[5] C. R. Paul, Inductance: Loop and Partial. New York, NY, USA: Wiley, 2010.

[6] C. R. Paul, "Prediction of Crosstalk in Ribbon Cables: Comparison of Model Predictions and Experimental Results," in *IEEE Transactions on Electromagnetic Compatibility*, vol. EMC-20, no. 3, pp. 394-406, Aug. 1978.

 