# *Root Cause Analysis and Defect Ground Effect of EMI Problem for Power Electronics*

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***Abstract*—The DC-DC converter is a crucial component of electronic modules or systems, and thus making electromagnetic interference issue essential. Even though power IC manufacturer often provides useful PCB design guidelines, but power electronic engineer sometimes ignores the design rules because of his own application concerned or cost issue. This usually leads the converter to a poor EMI performance in the first time, thus requiring additional engineering resources, greater time to market, as well as higher EMI filter costs to comply with related EMI regulations. In this paper, we'll analyze the root cause of EMI problem on a DC-DC converter module built with single layer-double side PCB, and point out some factors of PCB ground design that will affect the EMI performance. Since there is no complete pair for power-ground plane, the plane resonance issue will not be discussed in this paper.**

***Keywords— DC Converter ; EMI regulation; PCB Design***

## I. INTRODUCTION

The use of DC-DC converters is increasing in almost every industrial section and electronic product. As electronic systems have been more miniaturized, mobile, and complicated, the power requirements become more varied on different functional circuits. As product requirements constantly drive performance improvement and size reduction, EMI performance to meet related product standards [1][2] and authority regulations [3] requirement is crucial for every market.

Not only is the market for purchased converters growing, but also many circuit designers now design their own DC-DC conversion circuits on board instead of relying on power supply providers. Basic DC-DC conversion circuitry is fairly mature technology and continues to evolve rather slowly. Because of this it has become quite practical and important for designers to strengthen EMI design technique by analyzing possible root cause of EMI problem and creating regulation-compliance converter. The allowing radiated EMI emission limits for various product standards and regulations at 10m distance are shown in Fig. 1.

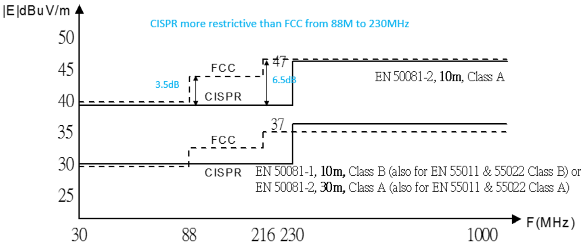


Fig. 1. EMI Emission Limits of Standards and Regulations for 10m distance: FCC CFR 47 Part 15B; CISPR 22/32：Class B for Residential

In this paper, some simulation challenges for EMI root cause analysis of an USB 5V charger with a boost DC-DC converter IC, from 3.7 V to 5 V are described. The assessed EMI design issues are the followings:

1. How to reproduce the radiated EMI problem of measurement by simulation?
2. What would be the noise source or cause resulting in the EMI problem, for example, is the ringing waveform at Lx point in Fig. 2 really the root cause of this case?
3. How to figure out the EMI debugging strategies with ANSYS simulation flow?
4. What would be the effect of attached USB cable on EMI emission?
5. How to deal with the trade-off between simulation time and far-field accuracy using simplified cable model, such as utilizing SIwave (2.5D Hybrid solver) near-field data linked to HFSS (3D full-wave solver)?

## II. EMI PROBLEM OF THE SWITCHING POWER SUPPLY

Simply stated, the function of a DC-DC converter is to provide a stable dc output voltage from a given input voltage. Ideally the dc output is to be “clean”, that is with ripple current or voltage held below a specified level. Furthermore, the load power is to be delivered from the source with some specified level of efficiency. The most common VRM for battery-powered product is the non-isolated synchronous boost topology as shown functionally in Fig. 2.

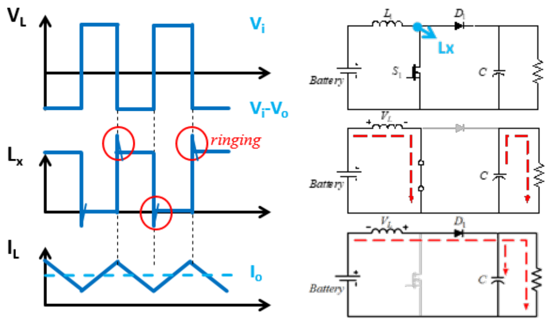


Fig. 2. Functional schematic of Boost DC-DC Converter and waveforms

The general tendency is to be concerned with the EMI generated at the switching frequency. Much of the EMI, and often the largest EMI signals, are not due to the switching but due to circuit resonances [4], such as PCB layout or cable attached.

The case study for this EMI root-cause analysis is an USB 5 V charger with a boost DC-DC converter IC. The device under test is supplied from 3.7 V input and then boosted to 5 V output to drive a 1 A current resistor load via an 87 cm long USB cable. The result of the radiated EMI test converted to 10 m distance for compliance check is shown in Fig. 3.

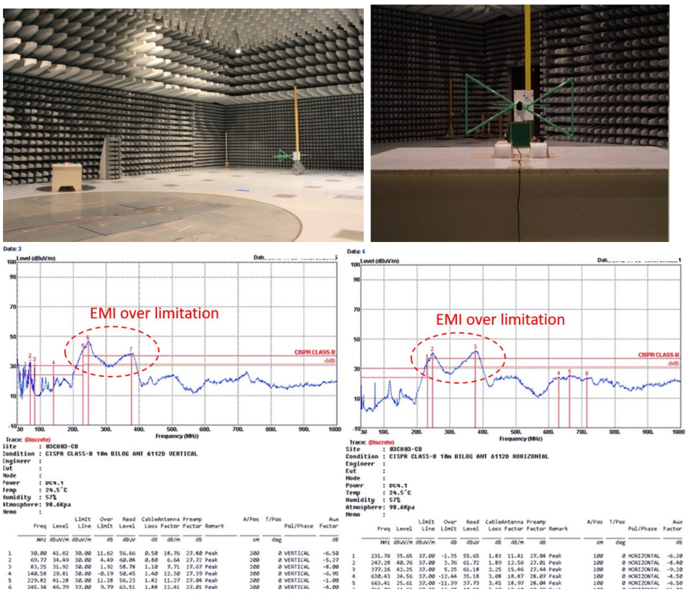


Fig. 3. 3 m converted 10 m Far-field EMI testing results

Since the EMI test results shows electric field level on some frequencies violating or over the emission limit of standard or regulation (peak frequency of the energy mountains at 250 MHz and 380 MHz). We thus measure the waveform of the Boost DC-DC Converter at the Lx depicted in Fig. 2 to further analyze if the ringing of Boost DC-DC Converter is the cause responsible for the EMI problem and peak emission observed in the far field. The measured waveform at Lx of the converter is shown in Fig. 4.

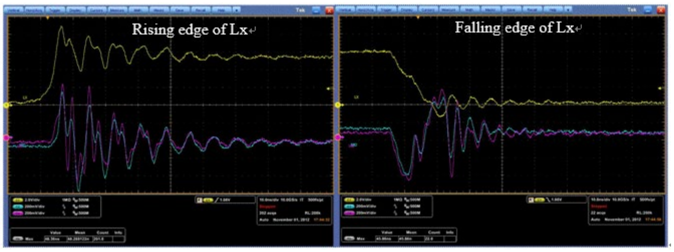


Fig. 4. Measured Lx waveform

The ringing period at Lx rising edge is about 8~8.5 ns, and the ringing period at Lx falling edge about 5.5~6 ns. Both of they don't seems consistent to the EMI tones, which are 250 MHz and 380 MHz.

## III. ROOT CAUSE ANALYSIS OF THE CONVERTER EMI PROBLEM

To characterize if the EMI violating frequencies relate to or depend on the ringing of Lx waveform, a parameterized simulation tool from ANSYS software is utilized for this analysis. The simulation parameters include the common mode signal component from broken PCB plane, RLC component model, and the radiation path with attached USB cable for the EMI problem reproduced to be consistent with tested result. Fig. 5 shows the top layer of PCB layout with power IC and decoupling capacitors for this simulation.

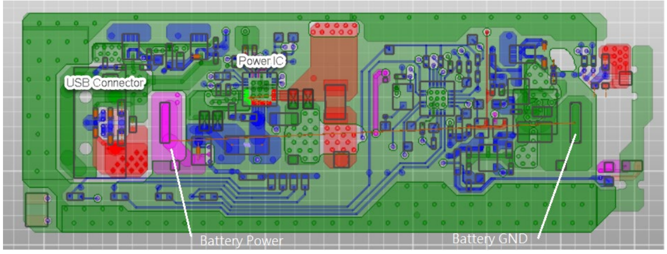


Fig. 5. The simulation PCB top layer layout with power IC and capacitors

However, we find out that even the measured Lx ringing phenomena could not be reproduced from the simplified simulation condition, the radiated EMI of simulation still matched the measured result. Here, we keep the simulation distance for EMI evaluation at 3 m for validation on EMI performance improvement, and thus do not convert to 10 m distance result for compliance check.

We thus further consider a more accurate RLC lumped model of power inductor downloaded from manufacturer's website [5], and consider the package parasitic effect as well in the next simulation.

We further consider the parasitic inductance effect of package not only on Lx but also ground path in Fig. 6, and compare the MOS gate drive frequency and duty cycle to 752 MHz/40 %, 852 MHz/40 % at Vin = 3.7 V respectively to investigate the effect of switching frequency and duty cycle. We find out that the higher duty cycle of switching resulting in more severe EMI emission, however the appearance of the ringing noise still does not affect EMI results as shown in Fig.

7. Therefore, we conclude that the ringing of Lx waveform is not the root cause of EMI problem.

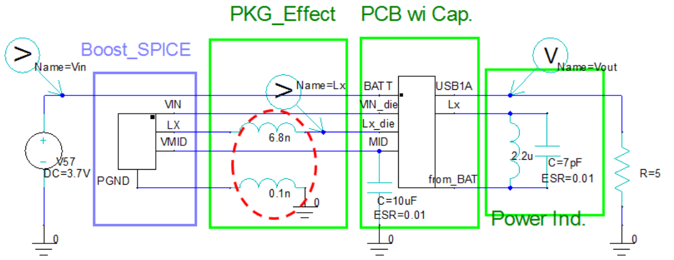


Fig. 6. Modeling with ground path inductance and larger Lx parasitic inductance of package

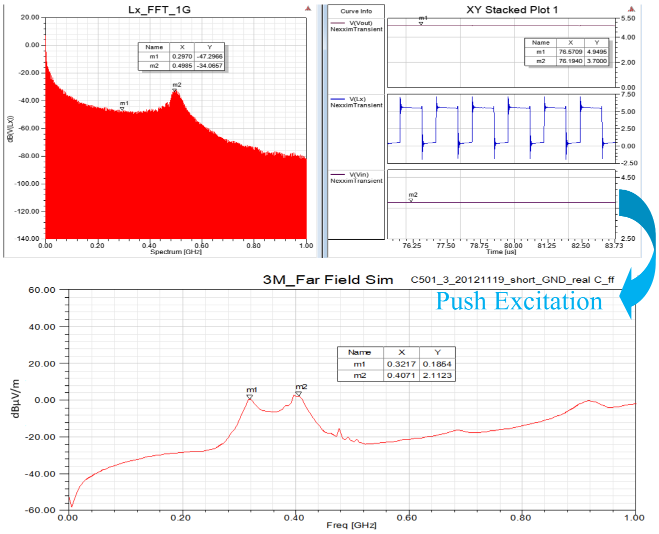
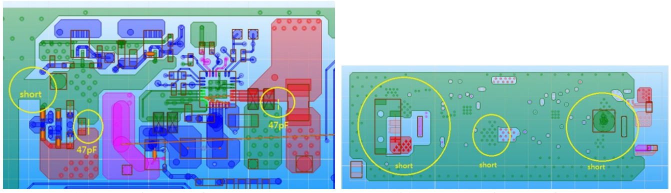


Fig. 7. EMI result linked from Lx waveform with ringing ($V_{in}$=3.7 V, MOS gate-drive frequency/duty cycle: 752 MHz/40 %)

Since we observe that the ringing of Lx waveform is not the root cause of the EMI problem from previous analysis in Fig. 6 to Fig. 7, we next investigate if the common mode noise induced from PCB layout is the root cause for this problem.

We then focus the current flow distribution and impedance on power and ground plane of PCB. Add two 47 pF decoupling capacitor, and short out some separated ground planes shown in Fig. 8 to search the root cause for this radiated EMI problem.



(a) Top layer of PCB (b) Bottom layer of PCB

Fig. 8. Layout of power and ground plane on PCB with different onfigurations

The improved EMI simulation result (green line) is shown in Fig. 9, and it does show the significant improvement with reduced electric filed peak values.

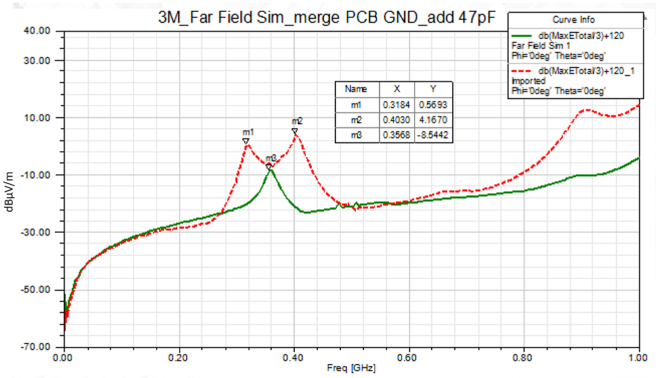
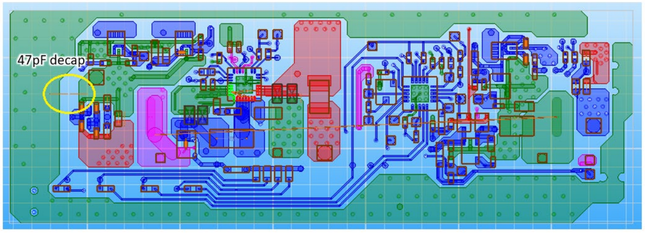


Fig. 9. EMI result after design strategies (adding a 47 pF capacitor and combine with different ground nets)

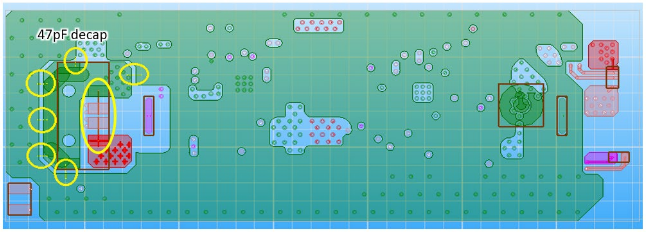
## IV. EMI DESIGN STRATEGIES AND VALIDATION

There are some applications of DC-DC converters that need to split grounds, and we then should provide bridging capacitors connecting the split planes as the second solution of EMI suppression. Therefore, we further implement the reconfigure reference plane and optimal high frequency decoupling capacitor placement to investigate the improvement to EMI performance.

Since the use of 47 pF high frequency decoupling capacitor is ineffective on resolving the EMI problem of split or separated ground layout due to system design consideration, especially when there exists a switch between separated grounds with its inadvertently $R_{on}$ effect. Therefore, we implement the design strategies with both adding 47 pF decoupling capacitor on USB 5V-to-GND and HF capacitor 47 pF crossing different ground plane as illustrated in Fig. 10, and we then obtain the results showing improved EMI performance in Fig. 11.



(a) Decoupling capacitor implementation corresponding to Fig. 8 (a)



(b) Decoupling capacitor implementation corresponding to Fig. 8 (b)

Fig. 10. Add a 47 pF decoupling capacitor on USB5V-to-GND and HF capacitor 47 pF crossing different GND plane

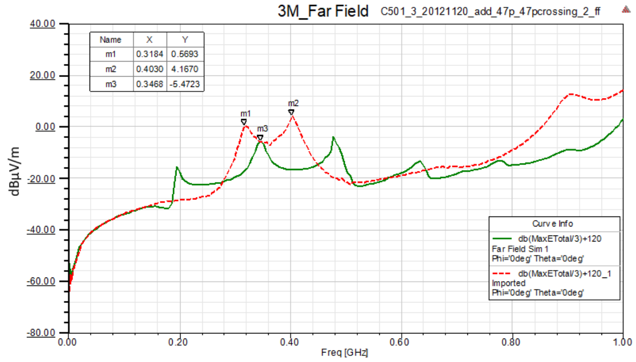
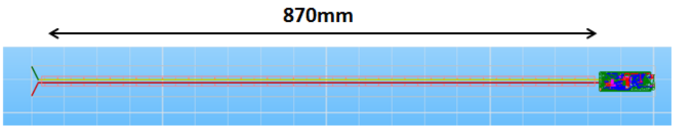
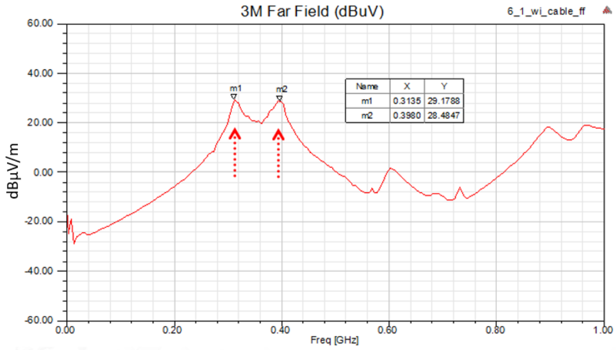


Fig. 11. The EMI result with both a 47 pF decoupling capacitor on USB5V-to-GND and HF capacitor 47 pF crossing different GND plane

Next, we draw a very long shielded trace pairs connecting USB5V and GND with 870 mm length, as shown in Fig. 12(a) in SIwave to simulate and analyze the cable effect on EMI emission. The result in Fig. 12(b) shows the emission level increasing 26 dB on dominant frequencies due to cable effect.



(a) Schematic draw of IC + PCB + USB Cable for simulation



(b) Far Field EMI with Cable attached

Fig. 12. Schematic and EMI Result for SIwave simulation for cable effect

Here we summarize the EMI results corresponding to each implementation in Fig. 13.

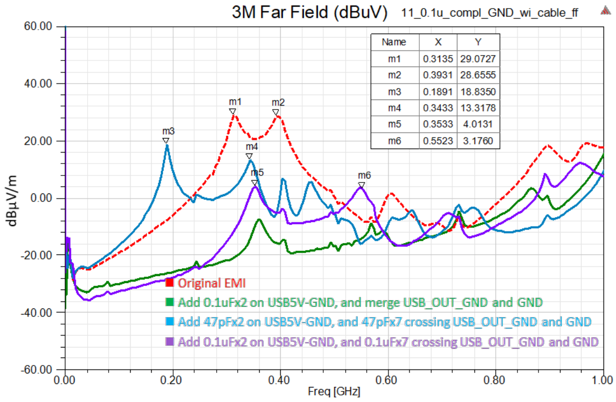


Fig. 13. EMI results under different configuration (all cable attached)

We thus identify the root cause to this radiated EMI emission of DC-DC converter is the common mode current appearing on attached cable generated by the broken and separated ground plane on PCB. Therefore, the problem could not be resolved by just adding the high frequency decoupling capacitor.

## V. CONCLUSIONS

The purpose of this paper is to provide EMI design insight with a simulation methodology based on measurement validation for design engineers working on power electronics to meet regulation compliance. Therefore, we have investigated many factors that maybe the causes affecting EMI performance of the boost DC-DC converter, as well as the possible solutions and common issues related to its EMI design. We have also pointed out a pitfall of common PCB layout leading to EMI problem from common mode current, and then provide improvement to the current path compensation with adequate capacitor which greatly improves the EMI performance. Recommendations for the DC-DC converter ground plane layout and simulation flow utilization was made to predict EMI performance and analyze root causes for further improvement.

Larger companies may be able to obtain the detailed model information of design module from the power IC component manufacturers, while smaller companies may need to rely on the measurement of several characterization boards to determine reasonable EMI design. Therefore, power electronic engineer can only estimate the rough trend of EMI performance but not absolute emission level. To achieve more accurate simulation result corresponding to test result, the detailed and accurate power IC model, package, USB connector, USB cable, and wide-band capacitor/inductance models are needed.

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