Reduce Radiation of PCIe Gen3 / 4 Signal by Common Mode Filter Design

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***Abstract*—Common mode filter constructed by ground plane voiding had been researched and verified in this paper. EMI test results shown radiation magnitude is reduced at target frequency with designed common mode filter. SSC (Spread Spectrum Clocking) is extensively used for PCIe signal to reduce radiation magnitude. While, SSC will not always be allowed in some PCIe3 configurations. Practicable design of common mode filter is essential to reduce radiation magnitude when system turns off SSC. This paper develops method to design common mode filter in PCB. This method had been verified by EMI test of actual system.**

Keywords—***PCIe 3, PCIe 4, SSC, Radiation, Common mode filter***

I. INTRODUCTION

This paper starts with an EMI test results of system operating with PCIe signal linkage turning off SSC (Spread Spectrum Clocking [1]). And, near field tests are performed to verify and understand mechanism of radiation for differential signals. In general, radiation caused by common mode current of differential signals will dominate [1][2].

In order to reduce radiation, mixed mode s-parameter formula is reviewed. For common mode to common mode s-parameter, we could increase coupling terms to reduce common mode to common mode s-parameter magnitude. With this as foundation, we could design ground plane voiding structure [3] which will cause destructive interference at target frequency for return current of differential signals. When return current can't go through ground plane, it will use nearby conductor as new path. And, this will increase coupling magnitude within differential pair and reduce the magnitude of common mode to common mode transition.

EDA tool is used to verify our idea by simulating s-parameter of differential traces with ground plane voiding structure. Finally, we fabricate board with designed common mode filter and performed both EMI and near field tests to verify effectiveness of methodology discussed in this paper. And, this method is also applied on PCIe 4 signal test board to validate for feasibility of application to reduce PCIe 4 signal radiation.

II. CASE STUDY OF SYSTEM RADIATION

Spread Spectrum Clocking (S.S.C.) is one methodology originally used to spread peak at spectrum of clock signal. To support SSC, PCIe transceiver chip needs to meet jitter requirement in common clock architecture [4]. When either transmitter or receiver can't meet the requirement, we would need to turn off SSC.

A. System radiation and near filed test.

It's expected that there will be peak at 4GHz when system transmitting with PCIe 3 (8Gbps data rate) signal. Fig1 is DUT system with SSC turning off, no peak at 4GHz is observed but 8GHz in EMI test. To further examine whether there is only 8GHz radiation for board design, we remove all chassis and perform near filed test at selected positions. While, we found similar phenomena at either connector or NVME cable as shown in Fig2.

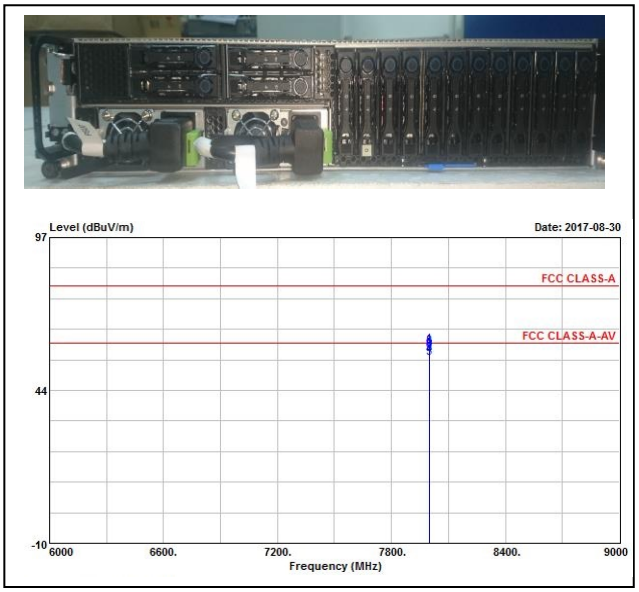

Fig. 1. DUT system with SSC turning off (top) and EMI test results (bottom).

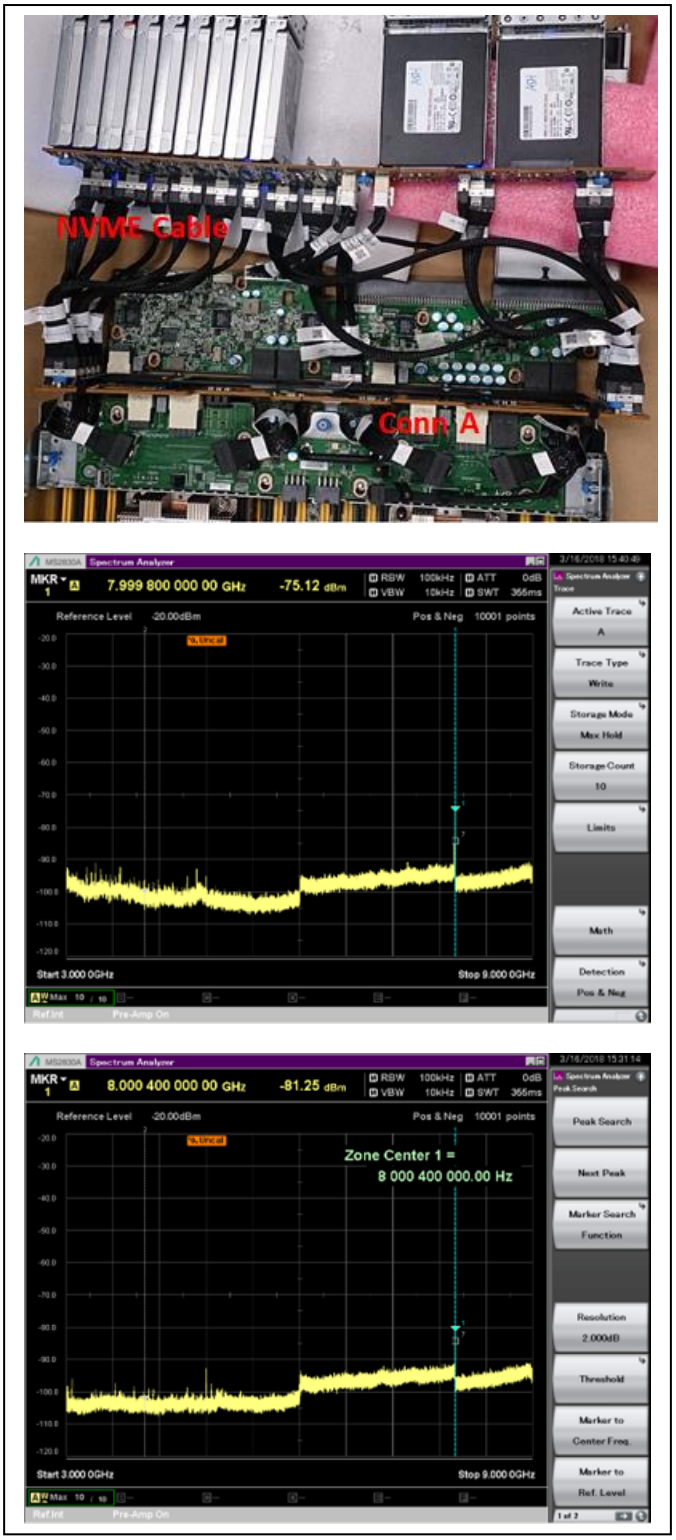

Fig. 2. System without chassis (top) and near field test results at Conn A (middle), and NVME Cable (bottom).

B. Radiation mechanism of differential signal

When signal transmitting through conductor of PCB, there will be corresponding return current in reference GND plane. When there is propagation skew between conductor pair of differential signals, summation of return current will not be zero and this will result in radiation as I_{C1} in Fig3. Similarly, there will be $I_{C1'}$ and $I_{C1''}$ having around 180 degree phase difference passing through connector pins. For receiving antenna, it will receive peak electrical field at time t1 from $I_{C1''}$ and at time t2 from $I_{C'}$. Since $I_{C1'}$ and $I_{C2''}$ have around 180 degree phase difference, observed peak electrical filed difference will be half of the period of original differential signals. That is, radiation frequency will be doubled when differential signal transmits through connectors. This is consistent with both EMI and near filed test results.

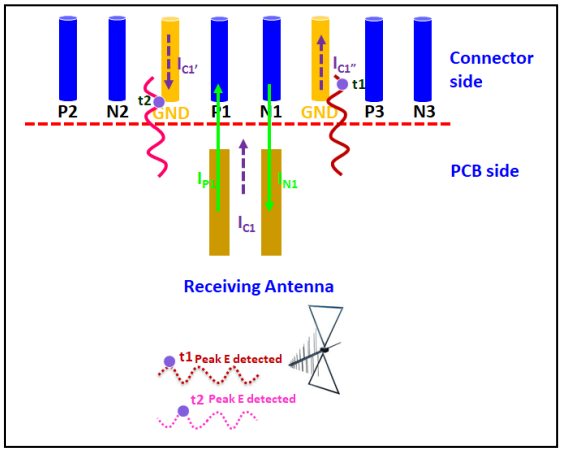

Fig. 3. Differential signals and radiation observed at receiving antenna.

III. Common Mode Filter Design Methodology

Equation (1) is common mode to common mode s-parameter S_{cc21} calculation for differential signal channel. Given input ports (1,2) and output ports (3,4), S_{31} and S_{42} are insertion terms and S_{32} and S_{41} are coupling terms. To reduce radiation, we need to decrease S_{cc21}. And, increase both S_{41} and S_{32} can achieve this goal since they are in reverse sign comparing to S_{31} and S_{42}.

$$S_{cc21} = (S_{31} + S_{42} - S_{32} - S_{41})/2 \quad (1)$$

A. Foundation of design methodology

When return current can't go through reference plane for differential signal, it will go through adjacent conductors. That is, the coupling between differential signals will increase and this could reduce radiation caused by common mode current. In Fig4, by designing path length L_{path},of GND voiding structure, there will be destructive interference for return current. Equation (2) shows relationship between L_{path} and target frequency f we would like to focus to reduce radiation. TD is signal propagation delay of path length in corresponding micro-strip or strip-line structure [2].

$$L_{path} = 1/(2 \times f \times TD) \quad (2)$$

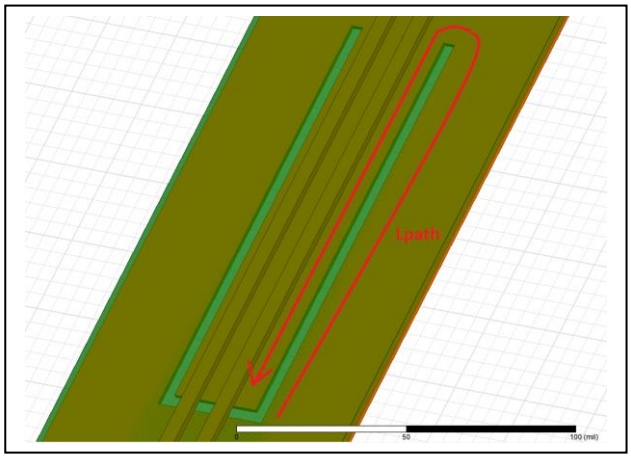

Fig. 4. Design of common mode filter by reference GND voiding.

B. *Simulation results*

Given target radiation frequency f is 8GHz and TD=1.4285*10^{-13} s/mil, L_{path}=437.5mil. Fig5. shows S_{cc21} simulation results comparison between differential signal channels with (green curve) and without (blue curve) u-shape void on GND reference plane. From simulation results, the structure will be common mode filter to filter out common mode to common mode transition close to 8GHz. And, this is close to our expectation since return current with 8GHz will encounter destructive interference under designed GND voiding structure.

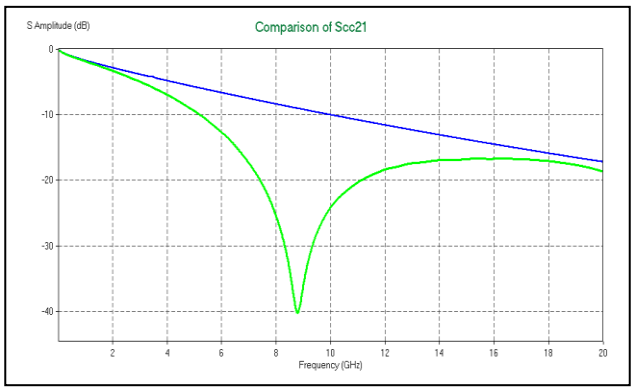

Fig. 5. Design of common mode filter by reference GND voiding.

C. *Implementation and Test Results*

Fig6 shows implementation example on actual PCB routing to solve EMI radiation issue in system of Fig1. Since the common mode filter design methodology only depends on reference plane voiding length, bending along with the differential signal trace will not change results. And, test results show that there is improvement for radiation peak at 8GHz. The design methodology is effective to reduce radiation at target frequency.

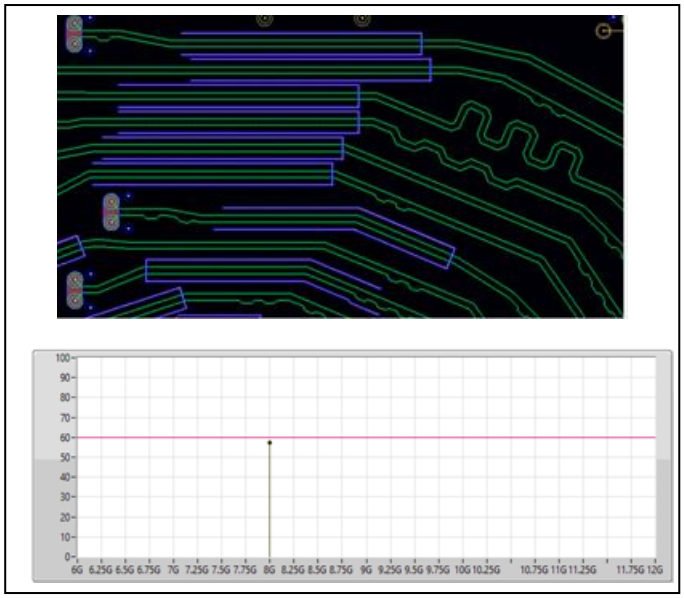

Fig. 6. Implementation in PCB routing (top) EMI test results (bottom).

D. *Validation for future PCIe 4 Application*

There is coming system design needs for PCIe 4 application. To study and solve EMI issue in advance, we had fabricated board with target frequency designed in 8GHz. Fig7 shows test setup for validation of effectiveness for PCIe 4 application. Pattern generator is used as PCIe 4 transmitter. The receive ends on this board are terminated with resistors to GND. Then, near filed probes connecting to frequency spectrum analyzer will measure at both PCB trace and cable side for boards with and without common mode filter design on them.

Fig8 shows test results comparison with and without common mode filter design for PCIe 4 data rate. Left top area is probe result at differential signal trace and there is radiation peak at 8GHz. Comparing with left top area, magnitude of right top one was reduced by 12.8dB. Left bottom area is probe result at cable linkage and there is radiation peak at 16GHz. Comparing with left bottom area, magnitude of right bottom one was reduced by 3.1dB.

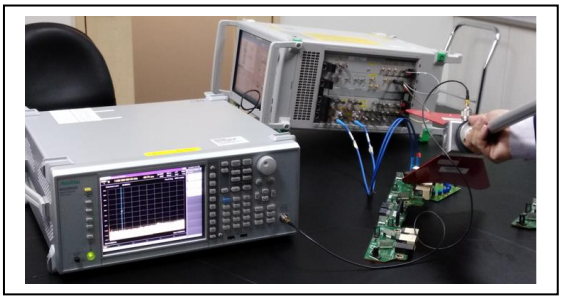

Fig. 7. Test setup for validation of common mode filter for PCIe 4 application.

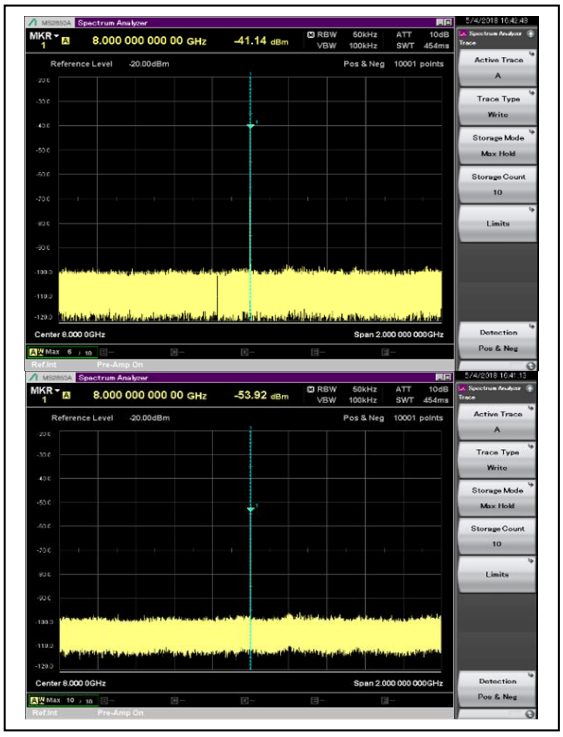

Fig. 8. Near filed probing at trace results comparison with (top) and without (bottom) common mode filter design for PCIe 4 data rate.

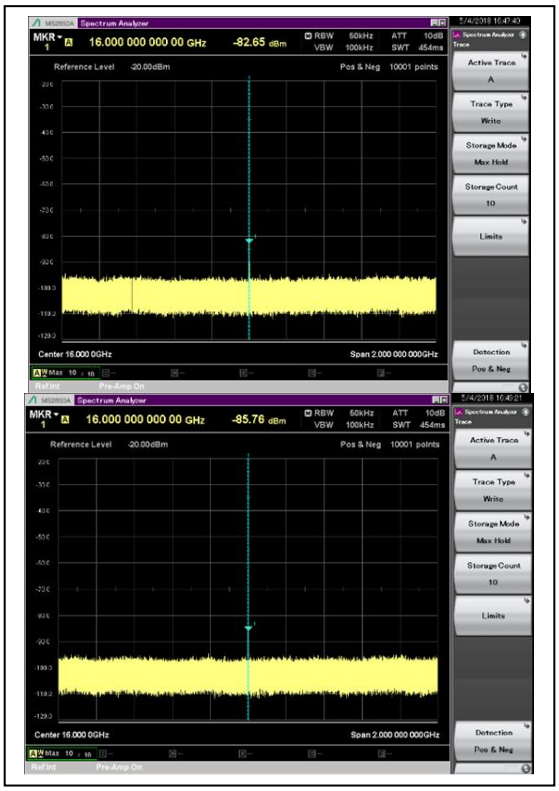

Fig. 9. Near filed probing at cable results comparison with (top) and without (bottom) common mode filter design for PCIe 4 data rate.

IV. Conclusion

Common mode filter design discussed in this paper can reduce radiation caused by common mode current of differential signals. And, target frequency is dependent on ground voiding path length and corresponding PCB construction. This design had been tested in actual system transmitting with PCIe 3 signals. With validation results of pattern generator transmitting 16Gbps signals, it could confirm that similar design methodology could be applied to future PCIe 4 application.

References

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