C-003

A Multiprocessor System for a Small Size Soccer Robot Control System

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1． Introduction

Recently, a multiprocessor system (MP for short) has actively researched. It possesses the benefit of increased performance and is promising in a lot of applications.

One of the applications is a soccer robot control system we have developed. Robot soccer contains many technologies such as mechanism designing, automated controls, LSI, wireless communication, artificial intelligence and so on. It has already become a hotspot in research field of robots. The idea of using multiple processors in the control system of soccer robots, is gaining popularity to perform different tasks and functions on different processors in embedded application. In this paper, a new fully digitized hardware design scheme of a soccer robot controller is presented as an application of a multiprocessor system. We will adopt an FPGA embedded multiprocessor systems, by which the hardware can be modified and tuned to provide optimal system performance easily. Experimental results show that our system is dependable, and has the characteristics of fast response and high precision.

2． Overview of a robot soccer game

A Small Size robot soccer game takes place between two teams of five robots each. The robots play an orange golf ball on a green carpeted field. By far the most common variety, use an overhead camera and off-field PC to identify and track the robots as they move around the field. An off-field PC is used to communication referee commands and position information to the robots. Communication is wireless and typically uses dedicated commercial units. The principle is shown in Fig.1.

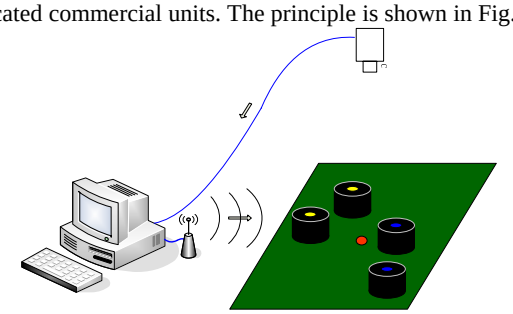

Fig.1 An image of the small robot soccer game[1]

3. Design of soccer robot control system

A soccer robot system can be divided into four subsystems, known as a communication, a decision, a vision and a robot subsystem. This report mainly describes the designing of the robot control system.

3.1 Previous control system

A DSP and FPGA based digital control system has already developed where FPGA gathers the data, and DSP computes with it[2]. Fig.2 describes the frame of the old system. This hardware architecture takes the advantage of the higher computation load of DSP and the rapid process of FPGA[3]. However, the design process will be complicated by this control architecture. And there were many disadvantages in this system below.

- Long design period, hard design modification;
- Many chips, so that there are many supply voltage, wire congestion and large area;
- Many interface between two boards, so it tends to make mistakes.

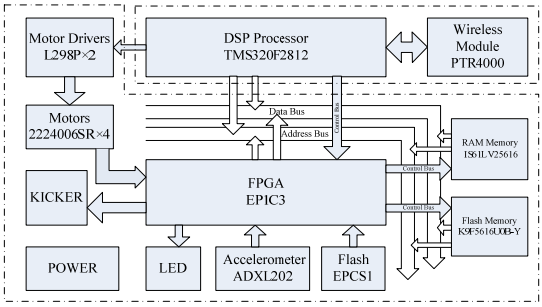

Fig.2 the DSP and FPGA-based digital control system[2]

3.2 New control system

To overcome the drawbacks of the previous system, a new system with embedded Nios II processors is developed.

3.2.1 Basic policy of system development

The new system is based on the Cyclone FPGA from ALTERA Corporation. Making use of SOPC (system on programmable chip) Builder tools, two 32 bit Nios II processors are integrated in FPGA, which can realize single-instruction 32*32 multiplication and division to produce a 32-bit result[4]. We developed the whole system and PID control segment by C-language, because C has the merits of easy programming and good real-time operation. But user defined components, such as PWM, wireless communication, speed sample and man-machine interface, are designed by using Verilog-HDL Language, so that they can be easily connected to the Nios II cores.

3.2.2 Control system design

There are many methods to partition the tasks and peripheral equipments of the control system for MP. The new system hardware architecture is shown in Fig. 3. It consists of two parts: a motors control part and a peripheral control part. The kernel of each part is a Nios II processor. One is used for the PID control of the motors. So that, motors have the real-time control that makes it respond quickly. The other one implements other functions of the control system, for example, wireless communication, states displaying, kicker controlling and accelerate sampling.

In the control part, using the MOS-FET circuit, processor 1 controls the four motors with the PID method. Each motor has a decoder, which can provide rotor position or speed information.

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Processor 1 can read this information from speed sample module via Avalon bus. Then it compares these values with the desired value in the RAM, and outputs control signals to the motor device.

Processor 2 communicates with PC by wireless module, samples the acceleration by ADXL202, and controls the kicker and LED. It gathers the information from PC and writes the data into the internal RAM. Then processor 1 fetches the data which is the desired value set by each control period.

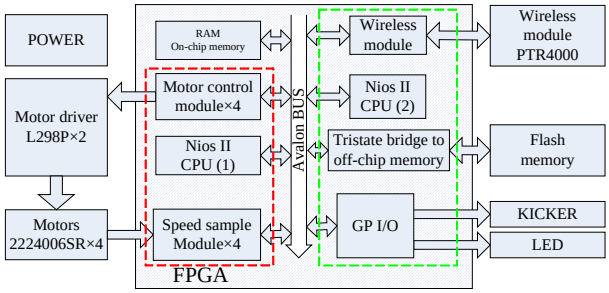

Fig. 3 hardware architecture of a new system

These two processors do not communicate with each other, but they use the same data in the RAM which connects with the Avalon bus.

Table I

The resources used in the controller

Family	Cyclone
Device	EP1C20
Total logic elements	5811/20060(29%)
Total memory bits	76,320/294,912(25.9%)
Total PLLs	1

We need not to consider the cache coherent problem because processor 2 uses ‘write through method’ while processor1 reads the data from the RAM each time. The resources used in the FPGA controller are shown in Table I.

3.2.3 Motor control module

Motor control is the key factor to improve the performance of the robot. A module for speed testing is designed by Verilog HDL language and incorporated in the system. The speed module prototype schematic is shown in Fig. 4.

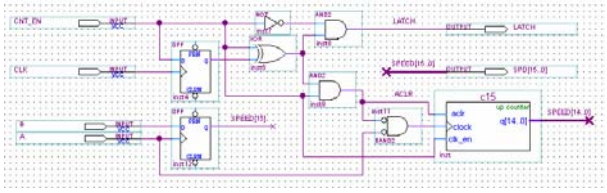

Fig. 4 the speed module prototype schematic

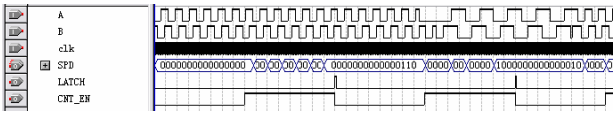

Fig.5 The simulation of speed module

For accurately, we use a 512 lines decoder attaching the dc-motor which outputs two phase signals. With the speed module, we can know how fast the motor runs and the direction. When the value of CNT_EN is zero, processor 1 can get the speed value via Avalon bus. The simulation wave form is shown in Fig. 5.

3.2.4 Wireless communication module

A soccer robot gets message from an off-field PC by wireless communication module. The communication should be fast, dependable, and it can resist jamming. In this design, nRF2401 has been selected, which is the industry's smallest, lowest cost, lowest current consumption and low voltage supply 2.4 GHz wireless RF transceiver. The nRF2401 runs on the ShockBurst™ mode which uses on-chip FIFO to clock in data at a low data rate and to transmit at a very high rate thus enabling extremely power reduction. When operating, we gain access to the high data rates (1 Mbps) offered by the 2.4 GHz band without another high-speed micro controller (MCU) for data processing [5].

3.3 Evaluation of the new System

Compared with the old control system (DSP & FPGA), there are many advantages in the new system. The total number of chip is decreased from 9 to 5, and the static current is also decreased. In the old system, we need two boards that one is DSP board, and the other is FPGA board. There are many interfaces between them. But in this new system, the time on drawing board is also decreased, because there is only one FPGA board that we need not to consider the interfaces.

Table II

Comparisons between two systems

	Previous System DSP &FPGA	New System FPGA
Chip count	9	5
Control period (ms)	2.17	1.59
Static current(mA)	542	227
PCB area(cm2)	219 (total)	127

※Designed by Protel 99.

4. Conclusions and future work

In this paper, a new high performance soccer robot control system has been developed as one of practical application of a multiprocessor system based on FPGA. It was successively realized, and experimental results for the speed control showed the feasibility of our FPGA-based multiprocessor system. Moreover, PCB area, which decides a total system size, can be decreased so that the robot is highly integrated.

Future work will be concentrated on optimizing the structure of the system and improving the speed PID control.

Reference

[1] http://www.robocup.org/
[2] Zh.Y.WU, C Li, L FENG. A Multi Micro-Motor Control System Based on DSP and FPGA. Small & Special Electrical Machines. 2007 Vol.35 No.1 P.30-32.
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[4] Altera Corporation, “Nios II Processor Reference Handbook”, The technology document of Altera company.
[5] Nordic Corporation, “nRF2401 Single Chip 2.4 GHz Radio Transceiver”, The technology document of Nordic semiconductor company.