IC-001 【既発表論文紹介】

Simulation-based Analysis of FF Behavior in Presence of Power Supply Noise

三浦 幸也† 山本 拓弥†
Yukiya Miura Takuya Yamamoto

出典：The 23rd IEEE International On-Line Testing Symposium (IOLTS 2017), pp.151-156

概要： 半導体デバイスの微細化，低電圧化により電源ノイズが回路動作に影響を与えることが問題になっている．特にメモリ素子（SRAM）ではビット反転の誤動作（エラー）が発生することが知られている．今後更にデバイスの微細化か進むと SRAM と同様の回路構造を持つフリップフロップ（FF）でも電源ノイズの影響が顕著になる可能性がある．本論文では FF においても電源ノイズによる SRAM と同様もしくは他の誤動作の発生の有無を解析した．その結果，ビット反転エラーおよびキャプチャエラーが発生するとこを確認した．またその発生原因を解明し，誤動作対策方法を提案する．

1. Introduction

In accordance with shrinking device sizes and lower-power supplies, of VLSI circuits, power supply noises have come to influence circuit behaviors. The bit-flip error of SRAM is well known as an influence on power supply noise [1]. The main cause of the error occurrence relates to sizes and threshold voltages of transistors in SRAM [2]. A FF circuit has a structure similar to SRAM. Therefore, when device sizes shrink, the lower-power supply and speeding up of VLSI circuits are further advanced, the problem mentioned above (e.g. bit-flip error) is also noticeable in the FF circuit [3].

This paper analyzes the behaviors of the FF circuit under several conditions including the threshold variation of transistors. This paper uses simulation-based analysis for investigating behaviors of FF circuits influenced by power supply noise. From analysis results, this paper also proposes countermeasures for errors. Note that we carried out the circuit simulation that gave the worst conditions (i.e., pessimistic scenario) to analyze the influence of power supply noise.

2. Analysis of FF circuits

For analyzing the behavior of the latch circuit, the Hspice simulator and 45-nm and 16-nm device parameters are used by changing simulation conditions: threshold variations of transistors and amplitude, duration and insertion timing of power supply noise [4]. Four D-FF circuits (FF1-FF4) are used for behavior analysis (i.e., transmission gate and clocked inverter types and two kinds of the connection node between master slave latches) (e.g., Fig. 1) [5].

From the analysis results, two kinds of errors are verified. One is the bit-flip error which means that the logic value held in the master latch is inverted by noise. The other is the capture error in which the slave latch captures an erroneous value because of the reduction of the output voltage of the master latch by noise.

Table 1 summarizes circuit conditions for error occurrences. The column “necessary” means necessary conditions and “combination” means other combinational condition. Error occurrences are deeply related to threshold variations at the loop part in the master latch circuit and noise generation around the clock edge. Analysis results and countermeasures of bit-flip errors are mainly shown in the following because of the page limitation.

† Graduate School of System Design, Tokyo Metropolitan University

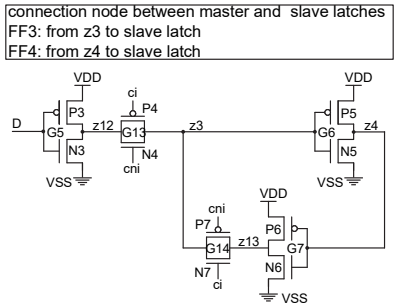

Fig. 1 Master latch of transmission gate type (FF3 and FF4).

Table 1 Conditions of error occurrences

Simulation conditions	Bit-flip error		Capture error	
	necessary	combination	necessary	combination
(1) FF type	-	FF1~FF4	-	FF1~FF4
(2) gates with variation	-	loop, master latch, whole	-	non-variation, loop, master latch, whole
(3) tr. threshold variation	G6=(fast, slow), G7=(slow, fast)	-	-	G8=(fast, slow), G8=(slow, fast), G8=(typical, typical)
(4) power supply for CK	-	same, different	-	same, different
(5) noise insertion point	-	master latch, whole	master latch	-
(6) noise amplitude	-	0.6~1.1 [V]	-	0.5~1.1[V]
(7) noise duration time	-	2~32 [ns]	-	7~32[ns]
(8) noise insertion timing	D={1, 0}, CK=rise	-	FF1,3:D=1,CK=fall FF2,4:D=0,CK=fall	-

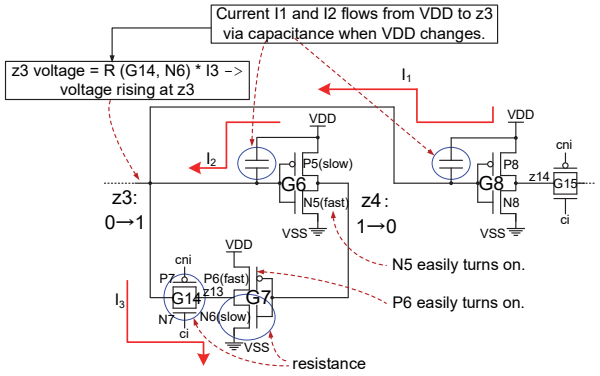

Fig. 2 Causes of bit-flip error.

When the logic value of z3 changes from 0 to 1 and the logic value of z4 changes from 1 to 0, the bit-flop error occurs. Two causes of the error are considered (Fig. 2). The first one relates to the rising voltage of the z3 node, which is caused when the power supply voltage returns to a normal voltage level. A current from VDD to z3 flows through parasitic capacitances of gate-source terminals of transistors P5 and P8 when the power supply voltage changes. The current flows to GND through gate G14 and transistor N6 of G7. At this time, both the flowing current and resistive components of gates on the current path cause a rising voltage of the z3 node.

The second cause relates to threshold variations of transistors. The threshold voltage of gate G6 is (nMOS, pMOS)=(fast, slow) and that of gate G7 is (nMOS, pMOS)=(slow, fast). Thus, N5 of G6 easily turns on, and the voltage of node z4 easily goes to a low level. Similarly, P6 of G7 easily turns on, and the voltage of node z3 easily goes to a high level.

The cause of the error, z3=1–>0 and z4=0–>1, is similar to the above.

From simulation results of 16-nm device parameters, those errors of 16-nm FFs occur easily under smaller amplitude and a shorter duration of power supply noise than 45-nm FFs, because the power supply voltage and the threshold voltage of 16-nm parameters are lower than those of 45-nm parameters. From those results, as shrinking of the device size proceeds, errors in FF circuits easily occur.

3. Countermeasures for FF error

The main cause of error, z3=0–>1 and z4=1–>0, is the voltage rising at z3 generated by the current from VDD to z3 through the parasitic capacitance and the resistive component of the gate. To prevent the error of, those values need to become small (Fig. 3). The size of gate G6 and/or G8 becomes small. Since this change results in the capacitance of G6 and/or G8 becoming small, the current from VDD to z3 becomes small. In addition, the size of gate G7 becomes large. Since this change results in the resistance of G7 becoming small, the voltage rising at z3 becomes small even if there is current flow. Moreover, since the drivability of G7 becomes strong, G7 preferentially produces a proper output value, and it becomes difficult for the error to occur.

For the error of z3=1–>0 and z4=0–>1, countermeasure is similar to the above.

Table 2 shows a performance comparison of countermeasure for the bit-flip error of z3=0–>1 and z4=1–>0. Comparing with the original FF design, transistor sizes to be large are modified to a double width and those to be small are modified to a half width. The effectiveness of those countermeasures was verified by circuit simulation. As a result, they do not cause the bit-flip error even if the maximum power supply noise is applied. Except for the delay time of FF3 consisting of transistors of a half size of G8, modified FFs show the almost same performances with them of the original FFs. Therefore, it is considered that proposed countermeasures are effective to prevent errors caused by power supply noise. Since transistor sizes of G8 in FF3 become small, drivability of G8 decreases. As a result, the propagation delay time of FF3 increases.

About other errors and other FFs including 16-nm FFs, transistor sizes were modified according to the method shown in this section. The effectiveness of those countermeasures was also verified by circuit simulation. As a result, all modified FFs never cause the error.

4. Conclusions

This paper analyzed the influence of power supply noise on FF circuit behaviors. Occurrences of the bit-flip error and the capture error were verified by circuit simulations, and their causes were clarified.

As countermeasures for the occurrences of those errors, adjustment of the drivability of gates by changing transistor sizes was effective. However, each countermeasure is effective for each error respectively and is not effective for other errors. The occurrence of the error depends on the current flow amount and the transistor size in the FF circuit. This means that the basic problem of the error occurrence is circuit structures in themselves of conventional FFs. Thus, as future work, development of FF circuits with new structures that can prevent malfunctions caused by power supply noise is needed.

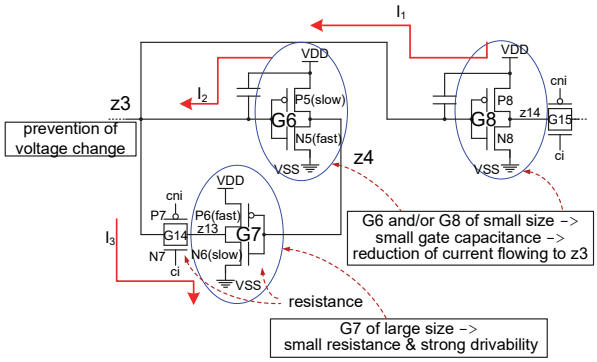

Fig. 3 Countermeasure for bit-flip error.

Table 2 Performance comparison of modified FFs

	Original FFs		Modified FFs		
	FF3	FF4	FF3	FF3	FF4
Gate (Tr.) size	-	-	G7=2W, G6=(1/2)W	G7=2W, G8=(1/2)W	G7=2W, G6=(1/2)W
Total width of Trs. [μm]	9.4400	9.1000	9.3757	9.3573	9.0175
Power consumption [μW]	131.98	132.08	132.01	131.92	132.04
Propagation delay (CK->Q), TpLH, TpHL [ps]	135.95, 131.00	86.81, 96.30	136.18, 130.95	160.31, 154.56	87.27, 97.39
ED product, ave. [μW*ps]	17616	12092	17631	20768	12191

Acknowledgment

This research was supported in part by Japan Society for the Promotion of Science under Grant-in-Aid for Scientific Research (C) (No. 25330068).

References

[1] M.-F. Chang and K.-A. Wen, “Power and Substrate Noise Tolerance of Configurable Embedded Memories in SoC,” The Journal of VLSI Signal Processing, vol. 41, no. 1, pp. 81–91, August 2005.
[2] T. Sawada, K. Yoshikawa, H. Takata, K. Nii, and M. Nagata, “Measurements of SRAM sensitivity against AC power noise with effects of device variation,” IEEE International Conference on Microelectronic Test Structures, pp. 77–80, March 2013.
[3] S. Nassif, V.B. Kleeberger, and U. Schlichtmann “Goldilocks Failures: Not Too Soft, Not Too Hard,” IEEE International Reliability Physics Symposium, pp. 2F.1.1–2F.1.5, April 2012
[4] Arizona State University, Predictive Technology Model (PTM) - http://ptm.asu.edu/
[5] NanGate Open Cell Library - http://www.nangate. com/?page_id=22