A Method for Aging Estimation of CMOS Circuits Using Ring Oscillators

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1. Introduction

The negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), and channel hot carrier (CHC) aging (degradation) of MOS FETs is one of the factors that reduces the performance of LSIs. Aging decreases the operating speed of a transistor, causing the LSI to ultimately malfunction due to increment in the signal propagation delay time. This paper presents a method for estimating the amount of increment in the delay time of an LSI and a method for estimating the amount of increment in the threshold voltage per transistor from the changes in the period of two ring oscillators by aging. Results of circuit simulations showed that the proposed methods can perform estimations with an error rate of less than 4.6 % for the delay time increment and less than 0.6 % for the threshold voltage increment.

Keywords: Aging (Degradation), Delay time, MOS FET, Ring oscillators, NBTI, PBTI, CHC

2. Aging estimation procedure

To estimate the aging of an LSI chip, the proposed method uses two kinds of ring oscillators (ROs) embedded in the LSI chip and utilizes their oscillation periods. First, we give an overview of the ROs. The RO is an oscillator consisting of odd numbered inversion-type gates that are connected like a ring. Its oscillation period corresponds to propagation delay time is within a design margin. When the delay time becomes large, resulting in the time margin becoming small, a warning signal is output. However, such methods can only measure the delay time of one pre-selected path. The method of [4] selects not only the critical path but also semi-critical paths at the design stage, and an embedded circuit can measure the propagation delay times of these multiple paths. However, the size of the measuring circuit increases as the number of measured paths grows. The method of [9] features ring oscillators (ROs) embedded in the LSI chip that are used to measure the propagation delay time influenced by MOS FET aging. This method uses two different ROs: one affected by PBTI, NBTI, and CHC and the other affected by PBTI and NBTI. Although this method can estimate the influence of aging for each kind of aging, it only estimates the amount of aging of MOS FETs used in ROs.

The above methods require the circuit for measuring the propagation delay time of a specific path(s) to be embedded at the LSI design stage. They cannot measure the propagation delay times of arbitrary paths increased by aging after LSI manufacturing. Under the long-term use of an LSI chip, the critical path frequently changes to another path because the increment ratio of the propagation delay time by aging is different for every path [10]. Therefore, it is necessary to measure the propagation delay times of multiple paths. In addition, the above methods cannot estimate the amount of aging at the MOS FET level. In this paper, we propose a method for estimating the delay time of the MOS FET, ΔtSD (increased switching delay), and the threshold voltage of the MOS FET, ΔVth (increased threshold voltage), both of which are increased by aging. We also propose a method for estimating the propagation delay time increased by aging, Δtpd (increased path delay), of any path in the LSI chip.

This paper is organized as follows. Section 2 outlines our proposed method for estimating a MOS FET aging and Section 3 describes circuit structures of ROs and their behaviors used for the aging estimation method. In Section 4, we describe the aging estimation method. Section 5 presents our evaluation and considerations of the estimation method by means of circuit simulations. We conclude with a brief summary in Section 6.

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the summation of the propagation delay times of all gates configuring the RO. The propagation delay time of a gate is determined by the delay time of the switching (i.e., switching time) behavior of the MOS FET. Thus, the oscillation period can be calculated from the switching time of the MOS FET. The switching time is calculated from an RC circuit model consisting of an on-resistance $R_{on}$ and a load capacitance $C$ of the MOS FET. An RC circuit model is used because it enables a simplified calculation model and the delay time can be calculated with relatively high accuracy. The switching delay time, $\tau_{sd}$, per MOS FET is expressed as [11]

$$
\tau_{sd} = 0.69 \cdot R_{on} \cdot C.
$$

(1)

The initial oscillation period, $T_{init}$, of the RO is expressed by

$$
T_{init} = 2 \cdot n \cdot k \cdot \tau_{sd},
$$

where $n$ is the number of gates and $k$ is a coefficient determined by a circuit structure such as a parallel connection or a serial connection of MOS FETs in the gate [11].

When both of the PMOS FET and NMOS FET experience aging, the threshold voltage $[V_{th}]$ of the MOS FET increases and then the on-resistance increases by $\Delta R_{on}$ [11]. When the on-resistance of the MOS FET increases by $\Delta R_{on}$ and the switching time per MOS FET increases by $\Delta \tau_{sd}$, the oscillation period of the RO from (1) and (2) is expressed as

$$
T = T_{init} + 2 \cdot n \cdot k \cdot \Delta \tau_{sd}.
$$

(3)

Two different kinds of ROs consist of gates provided by a standard cell library. Oscillation and non-oscillation modes of ROs can be switched by applying a control signal. Except for the measurement interval of the oscillation periods of ROs, the two ROs are always in the non-oscillation mode. In this setup, one RO is designed so that the PMOS FET does not receive the effect of the NBTI aging and the NMOS FET instead causes its own aging (NMOS-aged RO (i.e., PMOS-aging tolerant RO)) while the other is designed so that the NMOS FET does not receive the effect of the PBTI and CHC aging and the PMOS FET instead causes its own aging (PMOS-aged RO (i.e., NMOS-aging tolerant RO)) [13]. Therefore, as their aging is influenced only by either a PMOS FET or NMOS FET, $n$ MOS FETs receive their own aging during one oscillation period and the propagation delay time of the RO increases. Thus, the oscillation period of the NMOS-aged RO, $T_{n}$, is expressed by

$$
T_{n} = T_{init} + n \cdot k \cdot \Delta \tau_{sdn},
$$

(4)

where $\Delta \tau_{sd}$ is the delay time of one NMOS FET increased by its aging. The oscillation period of the PMOS-aged RO, $T_{p}$, is obtained in the same manner.

Next, we present the outline of the aging estimation method using the two ROs (Fig. 1). From (4), the increased delay time of one NMOS FET, $\Delta \tau_{sdn}$, is expressed by

$$
\Delta \tau_{sdn} = \frac{T_{n} - T_{init}}{n \cdot k}.
$$

(5)

The increased delay time of one PMOS FET, $\Delta \tau_{sdp}$, is obtained in the same manner. Therefore, $\Delta \tau_{sdn}$ and $\Delta \tau_{sdp}$ can be calculated from $T_{n}$ and $T_{p}$, which are the measurement values of the oscillation periods for the two ROs embedded in the LSI chip, and $T_{n_{init}}$ and $T_{p_{init}}$, which are the initial oscillation periods for the two ROs at the time of factory shipment (i.e., values without aging).

In the proposed method, the $T_{n}$ and $T_{p}$ oscillation periods of the two ROs embedded in the LSI chip are measured first (Fig. 1, S1). When the initial oscillation periods of these ROs (i.e., oscillation periods without aging), $T_{n_{init}}$ and $T_{p_{init}}$, are known, these periods are used for calculation. If the initial periods are unknown, they are calculated from a calculation model described in Section 3 and from the MOS FET parameters (Fig. 1, S2). Increased delay times, $\Delta \tau_{sdn}$ and $\Delta \tau_{sdp}$, are calculated from (5) by using those measured periods of ROs and initial periods (Fig. 1, S3).

The amount of the threshold voltage of the MOS FET increased by aging, $\Delta V_{th}$, is estimated second. Converting the equation of the calculation model for $\Delta \tau_{sd}$, which has the variable for the threshold of the MOS FET, generates the function of $V_{th}(\Delta \tau_{sd})$ (Fig. 1, S4). When $\Delta \tau_{sdn}$ and $\Delta \tau_{sdp}$ are applied to the function, the threshold voltage $[V_{th}]$ of the MOS FET in the LSI chip is obtained. Calculating the difference between those calculated values and initial threshold voltages (i.e., values without aging), the threshold voltage of the MOS FET increased by aging, $\Delta V_{th}$, is estimated (Fig. 1, S5).

Third, the obtained $\Delta \tau_{sdn}$ and $\Delta \tau_{sdp}$ are changed into the propagation delay time of the gate, $\Delta \tau_{gd}$, in the LSI chip increased by aging (Fig. 1, S6). A calculation model for all kinds of gates has been provided in advance. As the delay time of one gate depends on its own input value, the maximum delay time is assumed at the time of calculation. The number of fan-outs and the rising/falling time of the input signal are also considered for calculating the delay time. Applying the increased delay time of each gate obtained from the above to an arbitrary path in the LSI chip, the maximum delay time of the path, $\Delta \tau_{pd}$, increased by aging is estimated (Fig. 1, S7).

Figure 1 Outline of the aging estimation method.

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**Figure 1** Outline of the aging estimation method.
3. RO structures and their behaviors

Figs. 2 and 3 show two ROs [13]. In this paper, we explain the NMOS-aged RO (i.e., PMOS-aging tolerant RO). Fig. 2(a) shows the gate level diagram and Fig. 2(b) shows its MOS FET level diagram. The OR enters the oscillation mode when logic 1 is applied to control signal line 12 and enters the non-oscillation mode when logic 0 is applied to the control signal line. Fig. 2(a) also shows the logic values in the RO for the non-oscillation mode. MOS FETs used for oscillation are P11, N11, and N12 (see Fig. 2(b)). In the non-oscillation mode, P12 and N11 are on-state and P11 is off-state (i.e., P11 is not affected by the NBTI aging). By using the OR, therefore, it is possible to measure the oscillation period that is not influenced by the NBTI aging. However, the aging of N11 such as PBTI and CHC progresses. Similarly, when the RO consisting of NOR gates is used, a PMOS-aging tolerant RO (i.e., PMOS-aging tolerant RO) is realized (Figs. 3(a) and (b)).

![Figure 2](image1)

(a) non-oscillation mode  (b) MOS FET level

Figure 2 NMOS-aged RO.

![Figure 3](image2)

(a) non-oscillation mode  (b) MOS FET level

Figure 3 PMOS-aged RO.

4. Aging estimation method

In this section, we first explain the calculation model used for the aging estimation in detail. The oscillation periods of two kinds of ROs can be modeled by the RC circuit consisting of the $R_{on}$ and $C$ of the MOS FET. In the following, we discuss the model of the NMOS-aged RO as an example.

The on-resistance $R_{on}$ is calculated by [11]:

$$R_{on} = \frac{V_{ds}}{I_{ds}},$$

where $V_{ds}$ is the drain-source voltage and $I_{ds}$ is the drain-source current of the MOS FET.

$L_{ds}$ is given by the alpha-power low MOS FET model [12]:

$$L_{ds} = \frac{1}{2} \mu_{eff} \frac{V_{ox}}{t_{ox}} \frac{W}{L} \left(V_{gs} - V_{th}\right)^{\alpha} \left(1 + \lambda \cdot V_{ds}\right),$$

where $\mu_{eff}$ is the effective mobility, $V_{ox}$ is the dielectric constant of the gate oxide, $t_{ox}$ is the gate oxide thickness, $W$ and $L$ are the channel width and length, respectively, $V_{gs}$ is the gate-source voltage, $V_{th}$ is the threshold voltage, and $\lambda$ is the channel length modulation parameter. $V_{th}$ is calculated considering a substrate bias effect [14]:

$$V_{th} = V_{tho} + K_1 \left(\sqrt{V_{bs}} - \sqrt{V_s} - K_2 \cdot V_{bs}\right).$$

where $V_{tho}$ is the zero-bias threshold voltage. $K_1$ and $K_2$ are the body bias coefficient, $\Phi_s$ is the surface potential, and $V_{bs}$ is the bulk-source voltage.

The capacitance of the MOS FET, $C$, consists of a gate oxide capacitance $C_{ox}$, a junction capacitance $C_{jd}$, and an overlap capacitance $C_{gs}$ (i.e., $C = C_{ox} + C_{jd} + C_{gs}$) whose values are respectively calculated by (9), (10), and (11) (Fig. 4) [11]:

$$C_{ox} = \frac{\varepsilon}{t_{ox}} \cdot L \cdot W,$$

(9)

$$C_{jd} = \frac{c_j \cdot A_{sd}}{\left(1 + \frac{V_{s,d,pb}}{p_m}\right)} \cdot \frac{c_{js,d} \cdot P_{s,d}}{\left(1 + \frac{V_{s,d,pb}}{p_m}\right)} \cdot \frac{m_{js,d}}{m_{jsw}},$$

(10)

$$C_{gs} = C_{gd} = C_{gs} \cdot W = C_{gd} \cdot W,$$

(11)

where $c_j$ and $c_{js,d}$ are the zero-bias depletion capacitances of the bottom and sidewalls, respectively, $A_{sd}$ and $P_{s,d}$ are the area and perimeter of the source of drain implant, $p_m$ and $p_{msw}$ are the built-in potential for the bottom and sidewall components, respectively, $m_{js}$ and $m_{jsw}$ are the grading coefficients for the bottom and sidewall components, respectively, and finally $C_{gs}$ and $C_{gd}$ are the gate-source and gate-drain overlap capacitances, respectively.

![Figure 4](image3)

Figure 4 Capacitance model of the MOS FET.

![Figure 5](image4)

Figure 5 RC circuit model.

The oscillation period of the RO is obtained from the summation of the propagation delay time of each gate in the RO. Here, the propagation delay time is given by $tpLH$.
and \( tpLH \), which are the differences between input and output voltages when they reach up to 50% of the VDD.

Suppose the propagation delay times per gate in the NMOS-aged RO (PMOS-aged RO) are \( tpLH(n) \) and \( tpHL(n) \) \((tpLH(p))\). When the propagation delay times of \( tpLH(n) \) and \( tpHL(p) \) occur, only one MOS FET among two parallel-connected MOS FETs is in an on-state in the gate. Then, \( k=1 \) in (2) and its circuit model is as shown in Fig. 5(a). When the propagation delay times of \( tpHL(n) \) and \( tpLH(p) \) occur, both MOS FETs comprising the two serial-connected MOS FETs are in an on-state in the gate. Then, \( k=2 \) in (2) and its circuit model is as shown in Fig. 5(b). Therefore, the calculation model of the propagation delay time per gate of the NMOS-aged RO is expressed by [11]:

\[
\text{tpLH}(n) = 0.69 \cdot R_{on} \cdot \left( 2C_{dp} + 2C_{jn} + C_{gd} + C_{gs} + C_{gs} + C_{ox} + C_{gs} + C_{ox} + C_{gs} + C_{ox} + C_{gs} + C_{ox} \right),
\]

\[
\text{tpHL}(n) = 0.69 \cdot R_{on} \cdot \left( 2C_{dp} + 2C_{jn} + C_{gd} + C_{gs} + C_{gs} + C_{ox} + C_{gs} + C_{ox} + C_{gs} + C_{ox} + C_{gs} + C_{ox} \right),
\]

where symbols with the suffix \( p \) and \( n \) represent parameters for PMOS FET and NMOS FET, respectively.

As the summation of \( tpLH \) and \( tpHL \) is the propagation delay time per gate for one oscillator period, the calculation model for the oscillation period, \( T_{n} \), of the NMOS-aged RO is expressed by

\[
T_{n} = (\text{tpLH}(n) + \text{tpHL}(n)) \cdot n \cdot a,
\]

where \( a \) is a fitting coefficient for correcting the value of the oscillation period [15].

Supposing \( T_{n} \) is the oscillation period of the NMOS-aged RO embedded in the LSI chip (i.e., measured value), from (5), the calculation model of the increased delay time of one NMOS FET, \( \Delta sdn \), is expressed by (15). If the initial oscillation period, \( T_{n, \text{init}} \), of the NMOS-aged RO is known, its value is used for (15). However, if it is unknown, it can be calculated from (2).

\[
\Delta sdn = \frac{T_{n} - T_{n, \text{init}}}{2n}. \tag{15}
\]

Now, we explain the calculation method of \( \Delta V_{th} \) (the threshold voltage increased by aging). Suppose \( \Delta sdn \) and \( \Delta sd p \) are obtained from (15) and \( T_{n, \text{init}} \) and \( T_{p, \text{init}} \) are obtained from (2). In this case, the equations of \( \Delta sdn \) (\( \Delta sd p \)) can be expressed by the function with the variable of \( V_{th} \) as

\[
\Delta sdn = f(V_{th}) \cdot \Delta V_{th} = f(V_{th}). \tag{16}
\]

Converting (16), we obtain

\[
g(\Delta sdn, V_{th}) = 0. \tag{17}
\]

As \( \Delta sdn \) is a known value, (17) is a high-degree equation with the variable of \( V_{th} \). By solving (17), the \( V_{th} \) increase by aging is obtained. MATLAB is used for solving Eq. (17). Therefore, \( \Delta V_{th} \) is calculated by the difference between the estimated \( V_{th} \) from (17) and the initial \( V_{th} \) (i.e., without aging).

Next, we explain the estimation method of the maximum delay time of a path. The increased delay time of one NMOS FET, \( \Delta sdn \), obtained from (15) is first converted to the increased delay time of each gate used in the LSI chip. Suppose \( \Delta sd \) is estimated by (15) and \( \Delta V_{th} \) is estimated by (17). In addition, the increased delay time of each gate, \( \Delta tdg \), is calculated as the increased \( tpHL \) and \( tpLH \) by using the RC circuit considering the gate structure and the above \( \Delta sdn \) and \( \Delta V_{th} \). Then, a conversion coefficient \( w \) that converts \( \Delta sd \) (i.e., \( \Delta sdn \) and \( \Delta sd p \)) into the maximum increased delay time of the gate, \( \Delta tdg \), is calculated as

\[
w = \frac{\Delta tdg}{\Delta sd}. \tag{18}
\]

The gate delay time depends on both the transition time of the input signal (i.e., rising time and falling time) and the number of fan-outs (i.e., load capacitance) [11], [12]. For the influence of the transition time, the correction coefficient \( x \) is provided by

\[
x = \frac{\sum_{i=1}^{m} \Delta tdg_{a} \cdot \Delta tdg_{b}}{\sum_{i=1}^{m} \Delta tdg_{a}}. \tag{19}
\]

where \( \Delta tdg_{a} \) is the delay time for the input signal of a rectangular wave, \( \Delta tdg_{b} \) is the delay time for the input signal with a certain rising/falling time, and \( m \) is the number of the changed threshold voltage of the MOS FET instead of aging.

For the influence of the fan-out number, the correction coefficient \( y \) is provided by

\[
y = \frac{\sum_{i=1}^{l} \Delta tdg_{c} \cdot \Delta tdg_{d}}{\sum_{i=1}^{l} \Delta tdg_{d}}. \tag{20}
\]

where \( \Delta tdg_{c} \) is the delay time for the gate with a certain fan-out number and \( l \) is the number of the changed threshold voltage of the MOS FET instead of aging.

Thus, the maximum increased delay time \( \Delta tdg \) for each gate is calculated by

\[
\Delta tdg = \Delta sd \cdot w \cdot x \cdot y. \tag{21}
\]

From the above, as the \( \Delta tdg \) for each gate is obtained from the \( \Delta sdn \) of one MOS FET, the maximum increased delay time of any path, \( \Delta pdd \), in the LSI chip is calculated by applying \( \Delta tdg \) to gates on the path. For the estimation of \( \Delta tdg \), two approaches are considered. The first one calculates the path delay using the maximum increased delay time of the gate that does not consider its input value (method 1). The second one calculates the path delay considering the input value of the gate and the maximum value among \( tpLH \) or \( tpHL \) (method 2). In this work, we use both these methods in order to make the calculation as easy as possible.

5. Evaluation and considerations

In order to verify the effectiveness of the proposed methods, we carried out circuit simulations (HSpice) using 50-nm parameters [11]. The amount of aging is given by the increment of the threshold voltage, which was varied from 220 to 300 mV per 5-mV step. Table 1 shows the parameters of the MOS FET. The RO consists of 51 gates, the channel width of the NMOS-aged RO (NAND gate) is \( Wp/Wn=500 \text{ nm}/500 \text{ nm and} \)

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The method for estimating the path delay time is evaluated by using a two-bit adder consisting of two-input gates or three-input gates, which is a part of the standard logic circuit 74181. Fig. 8 shows the adder consisting of two-input gates. In the adder with three-input gates, the two-input gates in Fig. 8 are replaced with three-input ones. Table 3 shows the coefficients of \( w \), \( x \), and \( y \) used in (21).

![Figure 8 Two-bit adder (two-input gate).](image)

Table 3 Conversion coefficients.

<table>
<thead>
<tr>
<th>( w )</th>
<th>( b_{in} )</th>
<th>( b_{out} )</th>
<th>( x )</th>
<th>( 2\text{-fanout} )</th>
<th>( 3\text{-fanout} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOT</td>
<td>0.51</td>
<td>0.50</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>2NAND</td>
<td>1.93</td>
<td>2.22</td>
<td>1.5</td>
<td>1.3</td>
<td>1.6</td>
</tr>
<tr>
<td>2NOR</td>
<td>2.39</td>
<td>2.21</td>
<td>1.5</td>
<td>1.3</td>
<td>1.6</td>
</tr>
<tr>
<td>3NAND</td>
<td>2.73</td>
<td>4.35</td>
<td>1.5</td>
<td>1.3</td>
<td>1.6</td>
</tr>
<tr>
<td>3NOR</td>
<td>3.43</td>
<td>3.32</td>
<td>1.5</td>
<td>1.3</td>
<td>1.6</td>
</tr>
</tbody>
</table>

![Figure 9 Delay time of B1-S1 path.](image)

Fig. 9 shows the increased delay time, \( \Delta \text{tdp} \), of the path, B1-S1, containing the maximum number of gates. Table 4 summarizes the evaluation results for the estimation of the increased path delay time, where two kinds of paths are
selected: one with the maximum stage and the other with the maximum delay time. In method 1, the difference of the maximum increased delay time \( \Delta tpd \) between the estimated value and the simulated one ranges from -12.27 ps to +33.87 ps (error from -16.11% to +135.51%). In method 2, it ranges from -20.28 ps to +8.99 ps (-22.71% to +11.41%).

The reason the estimation result is higher than the simulation result is that the proposed method uses the maximum increased delay time of each gate. Conversely, the reason the estimation result is lower than the simulation result is that the load capacitance used by the calculation is smaller than that of the circuit used in the simulation.

Estimation results by method 1 are higher than those by method 2 because method 1 does not consider the input value and uses the maximum \( t_{pd} \) or \( t_{PLH} \) and \( t_{PHL} \). Therefore, in many cases, the value of \( \Delta tpd \) estimated by method 1 is higher than that by circuit simulation. In addition, the value of \( \Delta tpd \) estimated by method 2 is closer to that by circuit simulation.

Although we used two methods in this work for simple calculation, a more accurate estimation should be possible if an exact value applying to each gate, an exact gate size, and an exact load capacitance are used for calculation. However, the main purpose of this paper is to propose a method for estimating delay time with a reasonably good accuracy in an easy manner as possible.

6. Conclusion

Our main objective in this work was to estimate the delay time increased by aging with a reasonably accurate method that can be applied as easily as possible. We therefore proposed an aging estimation method that uses two kinds of ROs to enable the switching delay time \( \Delta tsd \) and the threshold voltage \( \Delta V_{th} \) per MOS FET increased by aging to be estimated. The path delay time increased by aging is also estimated using these values. Results of evaluation within the aging amount range of 80 mV showed that \( \Delta tsd \) can be estimated with an error rate of less than 0.13 ps and \( \Delta V_{th} \) can be estimated with an error rate of less than 1.7 mV. For the path consisting of eight stage of a two-bit adder, \( \Delta tpd \) can be estimated with an error rate of less than 20.28 ps.

In future work, we intend to develop a method incorporating the calculation of the load capacitance that considers circuit structure in order to elevate the estimation accuracy and an estimation method of the path delay time increased by real aging that considers the frequency of the gate usage.

Table 4 Summary of \( \Delta tpd \).

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Path</th>
<th>( \Delta tpd ) Method 1</th>
<th>( \Delta tpd ) Method 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-input adder</td>
<td>B0-S0: max stage</td>
<td>0.48 \pm 0.08 [19.50 - 32.64] ps</td>
<td>0.23 \pm 0.24 [10.34 - 20.58] ps</td>
</tr>
<tr>
<td></td>
<td>B1-S1: max stage</td>
<td>-2.54 \pm 0.96 [3.68 - 16.06] ps</td>
<td>-4.35 \pm 0.33 [10.01 - 8.78] ps</td>
</tr>
<tr>
<td></td>
<td>B1-C1: max stage</td>
<td>12.27 \pm 0.74 [16.11 - 2.58] ps</td>
<td>-20.28 \pm 1.45 [22.71 - 4.15] ps</td>
</tr>
<tr>
<td>3-input adder</td>
<td>B0-S0: max delay</td>
<td>-1.03 \pm 0.90 [25.97 - 23.88] ps</td>
<td>-1.22 \pm 5.30 [30.87 - 16.23] ps</td>
</tr>
<tr>
<td></td>
<td>B1-S1: max delay</td>
<td>0.16 \pm 6.02 [2.65 - 12.29] ps</td>
<td>-7.28 \pm 0.12 [9.09 - 0.32] ps</td>
</tr>
<tr>
<td></td>
<td>B1-C1: max delay</td>
<td>0.12 \pm 12.21 [3.28 - 24.44] ps</td>
<td>-0.88 \pm 1.07 [21.13 - 5.64] ps</td>
</tr>
<tr>
<td></td>
<td>B1-C1: max delay</td>
<td>1.35 \pm 11.18 [4.73 - 12.93] ps</td>
<td>-7.64 \pm 0.10 [18.84 - 1.86] ps</td>
</tr>
<tr>
<td></td>
<td>B0-S0: max delay</td>
<td>0.86 \pm 12.93 [6.73 - 17.41] ps</td>
<td>-6.59 \pm 1.07 [4.29 - 4.88] ps</td>
</tr>
<tr>
<td></td>
<td>B1-S1: max delay</td>
<td>2.87 \pm 33.87 [51.95 - 135.51] ps</td>
<td>0.65 \pm 6.38 [6.29 - 63.99] ps</td>
</tr>
<tr>
<td></td>
<td>B1-S1: max delay</td>
<td>0.71 \pm 12.87 [5.81 - 14.44] ps</td>
<td>0.48 \pm 8.99 [4.63 - 11.41] ps</td>
</tr>
</tbody>
</table>

References