RC-003

Dependable Techniques for Noise Block and Delay Variation Detection/Correction

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Abstract

Dual edge triggered flip-flops have been proposed for noise aware design. As the clock signal has two edges in nature, rising and falling edges, if an edge triggered flip-flop can sample data by using those two edges, the flip-flop has the highly ability to prevent sampling a noise signal on the data line. The dual edge triggered flip-flops have advantages that they do not require any additional signal and their application to existing synchronous digital circuits is easy. This paper shows new design of the dual edge triggered flip-flops improved a circuit size and performance. In addition, a method for signal delay variation detection and correction utilized the proposed flip-flop is proposed. We show effectiveness of proposed design and application to delay variation detection/correction by circuit simulation.

Keywords*: delay variation detection/correction, dependable design, edge triggered flip-flop, error and noise block, timing violence*

1. Introduction

According to scale-down of devise dimensions, reduction of a power supply voltage and speed-up of an operation speed by CMOS technology development, signal noises induced by energetic particles (e.g., soft errors) and by signal changes (e.g., crosstalk) come to influence circuit behaviors. For DSM VLSIs, errors by a single event transient (SET) become a serious problem as well as a single event upset [1]. The width of a SET pulse becomes wider, pulse propagation in the circuit becomes easy, and the pulse is sampled easy by flip-flops (FFs) as the operational frequency is higher. In addition, single event (SE) (e.g., single event transient) causes a crosstalk noise [2]. This effect is noticeable as the power supply voltage is lower, and the width of the crosstalk pulse increases as the power supply voltage is lower.

Since those signal noises caused by SE and internal signal changes are transient signal/voltage pulses, the circuit often results in a transient fault when the noise is sampled by FFs [3], [4]. Thus, in this paper, we focus the voltage pulse induced on the data signal line by multisource noise effects (e.g., SET and crosstalk). In order to prevent erroneous data sampled by FFs, several techniques have been proposed.

(1) Multiple data sampling method [3], [5], [6], [7]: In those method, two or more FFs sample data. The double data sampling method is a time and space redundancy method by using two FFs and two sampling times. If contents of two FFs are not consistent, the method produces an error signal. This method can detect error occurrence by on-line, but cannot correct it. The Razor method and the canary FF method are ones derived from this method [8], [9].
(2) Multiple redundancy method [10], [11]: In those method, dual modular redundancy or triple modular redundancy techniques are used to compare values in FFs. Those methods can block the glitch on the data line, but require additional control/clock signals.
(3) Noise reduction method [1], [12], [13]: In those methods, the amplitude of the noise signal is reduced by a masking/filtering effect. The reduction ratio depends on the value of RC product and the hysteresis property of the Schmitt trigger circuit. They may have the problem of the signal propagation speed, power consumption, and area overhead. In addition, their efficiency is unknown for the large pulse.

We have proposed a *dual edge triggered flip-flop* (*DET-FF*) for blocking the transient voltage pulse on the data signal line [14]. If data samplings are carried out by both the rising edge and the falling edge in the one clock period, the transient pulse occurred around single edge is never sampled and such the DET-FF can block the noise signal. The DET-FF does not require any additional clock/control signals and the noise width that the DET-FF can block is adjustable. In this paper, we show improved results of the circuit size and performance by the redesigned DET-FF.

In addition, the proposed DET-FF is applicable to delay variation detection and correction under the environment without noise generation because it can detect the inconsistency of data values at both edges. Furthermore, utilizing the warning signal of the DET-FF, the DET-FF can correct/mask the error/malfunction (e.g., delay fault) caused by signal delay, which is realized by inverting the FF output value. This means that the proposed DET-FF can provide the similar function with the Razor and the canary FF [8], [9].

The rest of the paper is organized as follows. Section 2 introduces the DET-FF. Section 3 presents the implementation example of the revised DET-FF. We show

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the effectiveness of the proposed FF through simulation results and observations. Application of the DET-FF to signal delay variation detection and correction under the environment without noise generation is presented at Section 4. Finally, we conclude this work in Section 5.

2. Dual edge triggered flip-flops

In this paper, we focus edge triggered flip-flops (ET-FFs) driven by a pulsed clock signal and transient voltage pulses on the data signal line induced by several noise sources (e.g., SET and crosstalk). We aim to prevent to sample such transient pulse as proper data by ET-FFs.

Signal noise and signal integrity problems are becoming one of serious issues for quality of DSM VLSI circuits. Signal noise will happen accidentally at any location, and will cause a transient voltage pulse on data lines. Prediction and prevention of signal noise occurrence is difficult because noise sources exist outside and inside of a VLSI chip and we usually do not have any way for calculating and solving their occurrence in VLSIs. We consider that signal noise will happen without intention and the prevention of influence caused by the noise in the circuit level is one of reasonable solutions for the measure against signal noise.

Conventional ET-FFs use only one edge, either the rising edge or the falling edge, to sample data, but not both. If the transient noise signal occurs on the data signal line and the signal occurrence satisfies the time constrains of the setup time and the hold time of the conventional, the ET-FF samples the noise signal as a proper data signal and it finally holds and outputs an erroneous value (Fig. 1, left).

In the following, for simple discussion, we assume that the clock signal and the noise pulse are the positive type and the data signal is positive logic (i.e., the active high level). The proposed method is applicable for the negative pulse and negative logic. In this paper we also assume the noise pulse of a rectangle wave form for simple discussion.

The clock signal has two edges into one period in nature, the rising edge and the falling edge. If data samplings are carried out by using both edges, the transient pulse occurred at single edge is never sampled and such the ET-FF can block the noise signal. We call such ET-FF a *dual edge triggered flip-flop* (*DET-FF*) [14].

If a data signal width is wider than the clock pulse width including the setup and hold times, the signal is proper data and the DET-FF samples/holds its value (Fig. 1, middle). If the width of the data signal is narrow than the interval between both edges, the DET-FF recognizes that the signal is noise because of inconsistency of data values at both edges (Fig. 1, right). The DET-FF does not sample the signal (noise) and its output holds the previous value. Therefore, by using the nature of the clock signal, the DET-FF can block to sample/hold erroneous data caused by transient signal noises. The DET-FF does not require any additional clock/control signals, any delayed elements, and any explicit duplication circuits. In addition, the width of the noise pulse we wish to block is adjustable if the width of the clock signal (or the timing of the rising edge or the falling edge) is changed.

The width of the data signal, *tdw*, must satisfy the timing constraint as follows:

Conventional ET-FF: $tdw \geq tsu + th$,

Proposed DET-FF: $tdw \geq tsu + th + tcw$,

where *tsu* and *th* are the setup time and the hold time, and *tcw* is the width of the clock pulse (Fig. 2). Thus the data duration time of the DET-FF becomes longer than that of the conventional ET-FF. This may be drawback of the proposed method.

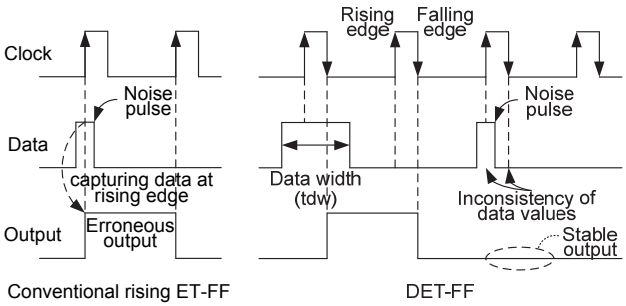

Figure 1 Basic function of dual edge triggered flip-flop.

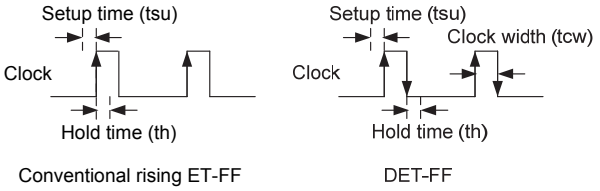

Figure 2 Time constraint.

Note that FFs called the double-edge triggered FF and the dual-edge triggered FF have been proposed [15]-[18]. Conventional ET-FF samples/holds data synchronizing single edge either the rising edge or the falling edge. On the other hand, those FFs use both edges to sample/hold each data signal, and then they can operate at half the clock frequency of conventional single ET-FFs. As a result, the method can reduce the power consumption. Therefore, this is a quite different technique with the proposed DET-FF.

3. Implementation of DET-FF

Considering the function of the DET-FF, there are four states between the clock signal and the data signal as shown in Fig. 3. When the data value at the rising edge is

the same as the data value at the falling edge (states (1) and (2) in Fig. 3), it is the proper signal. Then the DET-FF holds and outputs the signal. On the other hand, when the data values at both edges are different each other (states (3) and (4)), the DET-FF recognizes that the noise signal comes to the FF input and the DET-FF must hold the previous value.

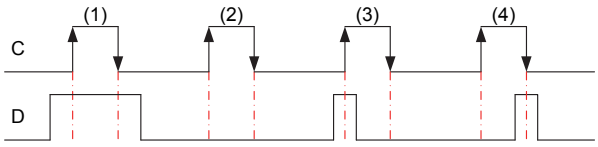

Figure 3 Relationship between clock signal and data signal.

Table 1 summarizes the function of the DET-FF. States (1) and (2) are the cases of proper data, the DET-FF holds/outputs the value of D reached at the FF input. The noise pulse reaches to the FF input (states (3) and (4)), the DET-FF holds the output value of the previous state. At this time, a warning signal plays the role of a flag to inform that the data signal at the rising edge is different from one at the falling edge. Then, the noise pulse on the data line is blocked, and the DET-FF is holding the previous value. For the other clock conditions (the last three rows in the table), the FF itself is in the hold state (state (Hold)), whose function is similar to conventional ET-FFs.

Table 1 Function table of DET-FF.

State	1st edge (Positive edge)		2nd edge (Negative edge)		Output		Warning
	C	D	C	D	Q	QB	
(1)	↑	1	↓	1	1	0	0
(2)	↑	0	↓	0	0	1	0
(3)	↑	1	↓	0	No change		1
(4)	↑	0	↓	1	No change		1
(Hold)	↓	X	↑	X	No change		0
(Hold)	0	X	1	X	No change		0
(Hold)	1	X	0	X	No change		0

The DET-FF that we proposed before has used the first stage circuit of the conventional ET-FF because they have good characteristics as an edge detector, however it resulted in a relatively large circuit. In this paper, we redesign the DET-FF so that it becomes smaller, low power consumption, and high speed.

Implementation example of a circuit satisfying the above function is shown in Figs. 4 and 5. The first stages of the proposed FF body sample data at the clock edge, and the second stage is designed for satisfying the function of Table 1. The upper part with the dashed line of Fig. 4 samples and holds the data signal at the rising edge, and the lower part samples and holds the data signal at the falling edge. In both circuits, the edge detection circuit consists of transmission gates, and latch circuits temporarily hold the data value sampled by the clock edge.

In order to satisfy the function of Table 1, two temporal holding values are compared each other, and the DET-FF outputs either the new sampled value or previous value based on the comparison result of consistency/inconsistency. In order to realize this function, the DET-FF uses the three-input Muller C-element for the output stage of the FF.

Until here, we assume the positive clock pulse. Exchanging C and CB of the C-element of Fig. 4, the DET-FF is applicable for the negative clock pulse.

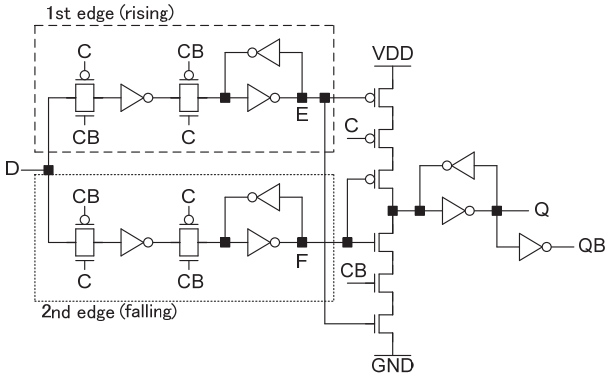

Figure 4 Dual edge triggered FF (body).

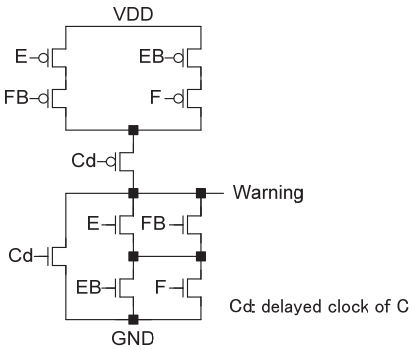

Figure 5 Warning circuit.

The warning circuit of Fig. 5 informs us that there is the noise pulse (i.e., the value at the rising edge is difference from one at the falling edge) producing the high level output. At this time, we know that the output of the DET-FF holds the previous value because of blocking the noise pulse. This function is realized by the combination of E, F, their inversion signals EB and FB, and the delayed clock Cd. If the delayed inverted clock CBd instead of Cd is used, the warning circuit can function for the negative clock pulse.

The function of Figs. 4 and 5 is verified by using 1.8 V 0.18-μm TSMC parameters. Table 2 summarizes characteristics of the DET-FF, where the combination of ET-FF means that the DET-FF function is realized by the combination of the positive ET-FF, the negative ET-FF, the comparator, and the multiplexor. Depending on a noise pulse type (positive or negative) and noise pulse generation timing, the DET-FF response differs. Values of [range] in the table mean the best value and the maximum value for each item. The circuit size (transistor count) of the redesigned DET-FF of this paper reduces to 58.3% of the previous DET-FF. The delay time and the power consumption also reduce than the previous one. Especially, the energy-delay product reduces to 51.7% than the previous one. Note that *tpQ*, *E*, and *ED* are measured by the following clock conditions: *T*(period)=3 ns, *tcw*=1 ns, *tr*=*tf*=0.01 ns.

The noise width that the DET-FF can block is determined by the clock pulse width *tcw*. If *tcw*=0.185 ns, the DET-FF can block surely the noise width between 0.168 ns and 0.185 ns (+*tsu*+*th*). Therefore, the minimum functional period T of the DET-FF alone is calculated as follows: *T*=*tcw*+*tsu*+max(*th*, *tpQ*, *tpW*)=0.78 ns. Then, maximum operating frequency is approximately 1.28 GHz

4. Signal delay variation detection and correction

In this section, we describe the application of the DET-FF to delay variation detection and correction. First of all, we assume the environment without noise generation in this section. We designed the DET-FF as a noise aware technique. In addition, the proposed DET-FF can find abnormal signal delay variation (i.e., abnormal signal transition) on the data line as follows. In the design policy of the DET-FF, the data signal must arrive before t he first edge of the dual-edge and must continue it until the second edge (see Fig. 6, (0)). Therefore, if a signal transition happens between two edges of the dual-edge, there is extra delay or too fast signal transition by some reasons. In this case, since signal values between the rising edge and the falling edge are different, the DET-FF can find it.

Figure 6 shows the relationship between dual-edge timing and data signal transition. In the normal signal transition (Fig. 6, (0)), the transition is done before the setup time of the first edge and its signal value continues until the hold time of the second edge. On the other hand, when a signal has an abnormal delay time (the slow transition delay fault of (1) and the path delay fault of (3)), signal transition occurs between two edges. Moreover, when signal transition is too fast (the fast transition delay fault of (2)), the transition also occurs between two edges. For those changes of transition timing, since the values of both edges differ, the DET-FF outputs the warning signal. Therefore, the DET-FF is utilizable for detection of abnormal delay variation. At this time, the width of a detectable delay time depends on the clock pulse width *tcw* as follows,

Slow transition (1) & path delay (3): $tsu < \Delta ds < tcw$,

Fast transition (2): $th < \Delta df < tcw$.

That is, when abnormal signal delay variation occurs by a certain reason and the signal transition occurs between two edges, the DET-FF can detect the abnormal delay variation (i.e., delay faults).

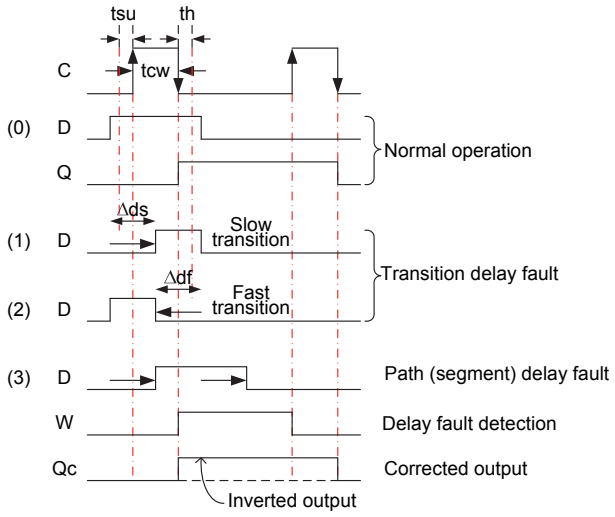

Figure 6 Relationship between dual-edge and signal transition.

Table 2 Characteristics of DET-FF.

		DET-FF [14]		combination of ET-FF		Proposed	
		max	[range]	max	[range]	max	[range]
# transistors (FF body)		60		84		32	
# transistors (warning)		12		(16) * a part of FF body		10	
minimum clock pulse width	tcw [ns]	0.351		0.358		0.185	
setup time	tsu [ns]	0.019	[-0.074, 0.019]	0.025	[0.008, 0.025]	0.123	[0.122,0.123]
hold time	th [ns]	0.106	[-0.080, 0.106]	0.048	[-0.098, 0.048]	-0.036	[-0.092,-0.036]
propagation delay of Q	tpQ [ns]	0.493	[0.342, 0.493]	0.701	[0.633, 0.701]	0.363	[0.347,0.363]
energy	E [pW]	3.120		1.319		1.775	
E*D product	ED [pW*ns]	1.303		0.880		0.673	
propagation delay of W	tpW [ns]	0.474	[0.429, 0.474]	0.502	[0.378, 0.502]	0.472	[0.434, 0.472]
minimum noise width	twn [ns]	0.231	[0.141, 0.231]	0.171	[0.100, 0.171]	0.168	[0.124, 0.168]
minimum noise amplitude	Vn [V]	1.008	[0.861, 1.008]	1.009	[0.865, 1.009]	1.131	[1.104, 1.131]

When signal transition occurs between two edges, the DET-FF outputs the warning signal, and the Q output signal also keeps the previous value. (Note that the conventional ET-FF also keeps the previous value because it cannot sample the input value.) Therefore, the DET-FF outputs a value opposite to the value that should be sampled and should be held. From this observation, when signal delay variation of Fig. 6 occurs, the signal value affected by the delay variation can be corrected by inverting the output value of Q intentionally (Qc of Fig. 6). In this method, it is better to make *tcw* as small as possible because of preventing signal delay increment by data correction. Figure 7(a) shows the example of a circuit for signal delay variation detection and correction that applied the DET-FF. We call the circuit a delay detection and correction (DDC) circuit.

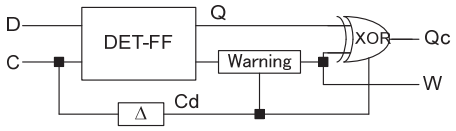

Figure 7(a) Delay detection and correction (DDC) circuit.

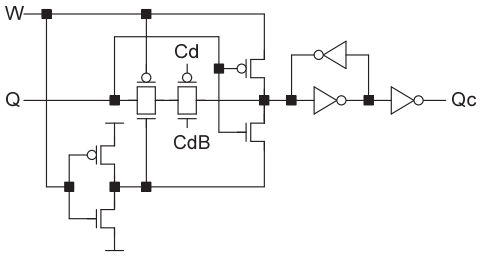

Figure 7(b) XOR.

Since the circuit of Fig. 7(a) determines inverting/non-inverting of the output signal by the value of the warning signal W, it uses the XOR gate. Conditions of the inverting output are W=1 and (W=0 & C=1). The warning signal retunes logic 0 when C=1, then the output signal is also inverted for the condition of (W=0 & C=1). For this purpose, the inverting/non-inverting function of the XOR gate is synchronized with the delayed clock signal Cd (Fig. 7(b)).

Figure 8 shows simulation results of the DDC circuit of Fig. 7(a), where from the top, the figure shows the clock signal C, the data signal D, the output signal Q, the warning output W, and the corrected output signal Qc. Rising transition to the logic 1 is delayed at (b), and fast falling transition occurs at (c), then the warning signal is outputted at (b2) and (c2). Thus, we find there is timing violence in the data signal. For both cases (b) and (c), the output Q holds the previous value ((b1) and (c1)). When the warning signal appears ((b2) and (c2)), W=1 and (W=0 & C=1) are held. Then, for these intervals, the output signal Q is inverted and the corrected signal Qc is outputted at (b3) and (c3). Thus, the DDC circuit of Fig. 7(a) can correct the delayed signal.

5. Conclusions

This paper showed the new implementation of the dual edge triggered flip-flop, DET-FF, which can block the noise pulse by using two edges of the clock signal. The DET-FF informs us that there is the noise signal on the data line by outputting the warning signal and the FF holds the previous value. The circuit size and the energy-delay product of the redesigned DET-FF reduced to 58.3% and 51.7% than the previous one, respectively.

In addition to noise pulse blocking, the delay detection and correction (DDC) circuit derived from DET-FF was applicable to delay variation detection/correction. The

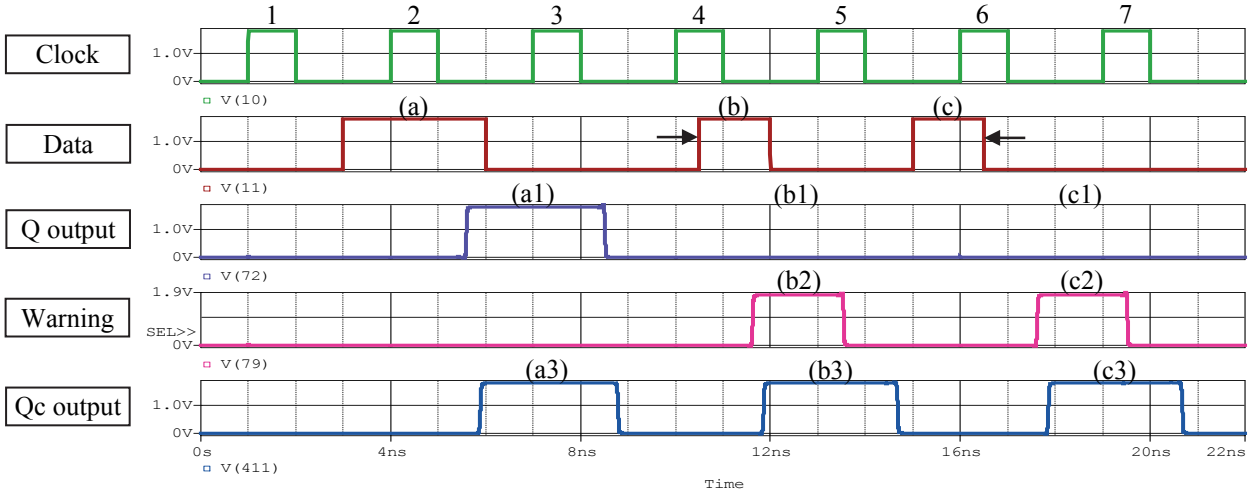

Figure 8 Simulation results of DDC circuit.

warning signal can play the role of delay detection, and the signal value affected by signal delay variation can be corrected by inverting the DET-FF output that is provoked by the warning signal.

If the clock signal of the DET-FF (DDC circuit) synchronizing with the set-up time and the hold time of the clock signal for the conventional ET-FF is provided (i.e., the first edge synchronizes with the set-up time and the second edge synchronizes with the hold time.), the DET-FF (DDC circuit) will detect violations of the set-up time and the hold time of the conventional ET-FF. It is necessary to clarify the relationship between a system clock and delay variation detection/correction as a future work.

The DET-FF used the delayed clock signal, which may become the problem of the power consumption. Measures for the power consumption will be necessary.

This paper considered the edge triggered FF. We will apply the similar idea to the level sensitive (master-slave) FF. In addition, a noise generation/evaluation method is needed in future works. We assumed the environment without noise generation for the delay variation detection/correction in this paper. The development of the dependable technique for both noise block and delay detection/correction is necessary in a future work.

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