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Dependable Dual Edge Triggered Flip-Flops for Bloking Noise Signal

Yukiya Miura [†]

Abstract

This paper proposes a dual edge triggered flip-flop for blocking a noise signal induced on data signal lines. The clock signal has two edges in nature, the rising edge and the falling edge. If an edge triggered flip-flop can sample data by using those two edges during one clock period, the flip-flop has the highly ability to prevent sampling the noise signal on the data line, comparing the conventional single edge triggered flip-flops. The proposed flip-flops have advantages that they do not require any additional clock/control signal and delay element to block the noise signal. Thus, their implementation/application to existing synchronous digital circuits is easy. Besides, the noise width that the proposed flip-flops can block is adjustable when the width of the clock signal is adjustable. In addition to noise signal blocking, they can apply to detection/correction of timing errors and delay faults. We show effectiveness of proposed design by circuit simulation.

Keywords: data signal, dependable design, edge triggered flip-flop, noise, single event transient, synchronous circuits

1. Introduction

According to scale-down of devise dimensions, reduction of a power supply voltage and speed-up of an operation speed by CMOS technology development, signal noises induced by energetic particles (e.g., soft errors) and by signal changes (e.g., crosstalk) come to influence circuit behaviors. For DSM VLSIs, errors by a single event transient (SET) become a serious problem as well as a single event upset [1]. The width of a SET pulse becomes wider, pulse propagation in the circuit becomes easy, and the pulse is sampled easy by flip-flops (FFs) as the operational frequency is higher. In addition, single event (SE) (e.g., single event transient) causes a crosstalk noise [2]. This effect is noticeable as the power supply voltage is lower, and the width of the crosstalk pulse increases as the power supply voltage is lower.

Since those signal noises caused by SE and internal signal changes are transient signal/voltage pulses, the circuit often results in a transient fault when the noise is sampled by FFs [3], [4]. Thus, in this paper, we focus the voltage pulse induced on the data signal line by multisource noise effects (e.g., SET and crosstalk), because we have already proposed noise blocking methods for the noise pulse on the clock signal line [5]. In order to prevent erroneous data sampled by FFs, several techniques have been proposed.

† Faculty of System Design, Tokyo Metropolitan University

(1) Multiple data sampling method [3], [6]-[8]: In those method, two or more FFs sample data. The double data sampling method is a time and space redundancy method by using two FFs and two sampling times. If contents of two FFs are not consistent, the method produces an error signal. This method can detect error occurrence by on-line, but cannot correct it. The Razor method and the canary FF method are ones derived from this method [9], [10].

(2) Multiple redundancy method [11], [12]: In those method, dual modular redundancy or triple modular redundancy techniques are used to compare values in FFs. Those methods can block the glitch on the data line, but require additional control/clock signals.

(3) Noise reduction method [1], [13], [14]: In those methods, the amplitude of the noise signal is reduced by a masking/filtering effect. The reduction ratio depends on the value of RC product and the hysteresis property of the Schmitt trigger circuit. They may have the problem of the signal propagation speed, power consumption, and area overhead. In addition, their efficiency is unknown for the large pulse.

In this paper, a dependable edge triggered FF based on a new concept is proposed, which can block the transient voltage pulse on the data signal line, and results in dependable design. The clock signal has two edges in one period, the rising edge and the falling edge. If data samplings are carried out at both the rising edge and the falling edge, the transient pulse occurred at a single edge is never sampled and such the ET-FF can block the noise signal. We call such ET-FF a *dual edge triggered flip-flop* (*DET-FF*). The DET-FF does not require any additional clock/control signals and the noise width that the DET-FF can block is adjustable.

The rest of the paper is organized as follows. Section 2 introduces the purpose of this paper. The dual edge triggered flip-flop is presented in Section 3. Section 4 presents an implementation example of the DET-FF. We show the effectiveness of the proposed method through simulation results and describe observations for simulation results in Section 5. Finally, we conclude this work in Section 6.

2. Purpose

In this paper, we focus edge triggered flip-flops (ET-FFs) and transient voltage pulses on the data signal line induced by several noise sources (e.g., SET and crosstalk). We aim to prevent to sample such transient pulse as proper data by ET-FFs.

Signal noise and signal integrity problems are becoming one of serious issues for quality of DSM VLSI circuits. Signal noise will happen accidentally at any location, and will cause a transient voltage pulse on data lines. Prediction and prevention of signal noise occurrence is difficult, because noise sources exist outside and inside of a VLSI chip and we usually do not have any way for calculating and solving their occurrence in VLSIs. We consider that signal noise will happen without intention and the prevention of influence caused by the noise in the circuit level is one of reasonable solutions for the measure against signal noise.

Conventional ET-FFs use only one edge, either the rising edge or the falling edge to sample data, but not both. If the transient noise signal occurs on the data signal line and the signal occurrence satisfies the time constrains of the setup time and the hold time at the rising edge or the falling edge, the conventional ET-FF samples the noise signal as a proper data signal and it finally holds and outputs an erroneous value.

If we use multiple data samplings to catch proper data, we can evaluate the width of the signal pulse (i.e., the signal having enough duration time (width), not the glitch). The clock signal has two edges (i.e., the rising edge and the falling edge) into one period in nature. If data samplings are carried out at both the rising edge and the falling edge, the transient pulse occurred at the single edge is never sampled and such the ET-FF can block the noise signal. We call such ET-FF the dual edge triggered flip-flop (DET-FF). The DET-FF does not require any additional clock/control signal, any delayed element, and any explicit duplication circuit. In addition, the noise width that the DET-FF can block is adjustable when the width of the clock signal is adjustable. Thus, by using the nature of the clock signal, the DET-FF can block to sample/hold erroneous data caused by transient signal noises.

Note that FFs called the double-edge triggered FF and the dual-edge triggered FF have been proposed [15]-[18]. Conventional ET-FF samples/holds data synchronizing the single edge either the rising edge or the falling edge. On the other hand, those FFs use both edges to sample/hold each data signal, and then they can operate at half the clock frequency of conventional single ET-FFs. As a result, the method can reduce the power consumption. Therefore, this is a quite different technique with proposed dependable FFs.

3. Dual edge triggered flip-flops

In the following, for simple discussion, we consider that the clock signal and the noise pulse are the positive type and the data signal is positive logic (i.e., the active high level). The proposed method is applicable for every combination of negative logic and positive logic between the clock signal and the noise pulse. In this paper, we also consider the noise pulse of a rectangle wave form for simple discussion.

The proposed DET-FF samples data by using both the rising edge and the falling edge. If a data signal width is wider than the clock pulse width including the setup and hold times, the signal is proper data and the DET-FF samples/holds its value (Fig. 1, left). If the width of the data signal is narrow than the interval between both edges, the DET-FF recognizes that the signal is noise because of inconsistency of data values at both edges (Fig. 1, right). The DET-FF does not sample the signal and its output holds the previous value. Therefore, the DET-FF can block the noise pulse. This method has advantages that any additional signals are not needed and the width of the noise pulse we wish to block is adjustable if the timing of the rising edge or the falling edge is changed.

The width of the data signal, tdw, must satisfy the timing constraint as follows:

Conventional ET-FF: $tdw \geq tsu + th$,

Proposed DET-FF: $tdw \geq tsu + th + tw$,

where tsu and th are the setup time and the hold time, and tw is the width of the clock pulse (Fig. 2). Thus the data duration time of the DET-FF becomes longer than that of the conventional ET-FF. This may be drawback of the proposed method.
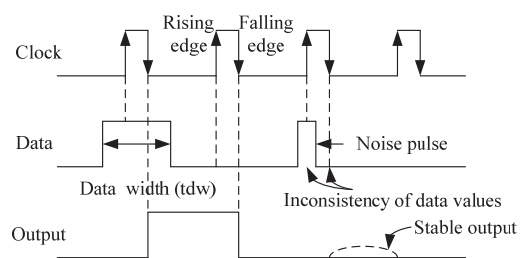

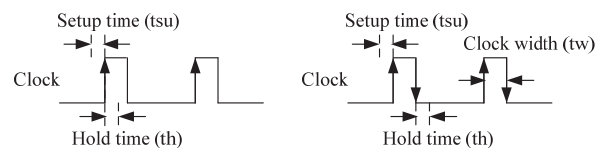Figure 1 Concept of dual edge triggered flip-flop.

Figure 2 Setup time and hold time.

4. Implementation

In order to implement the DET-FF as a realization example, we use first stage circuits of conventional ET-FFs because they have good characteristics as an edge detector. The second stage of the conventional ET-FF is the SR-FF. The left side of Fig. 3 is the conventional positive (rising) ET-FF and the right one is the first stage of the conventional negative (falling) ET-FF. In the positive ET-FF, when C=0, the first stage samples data, then, QMB=DB, QM=D. Here VB denotes the inversion of a logic value V. At this time, the second stage holds the previous state. When C goes to the logic 1 (0 -> 1), values

of QMB and QM propagate respectively to Ep and EpB through inversion gates, then Ep=D and EpB=DB, and the FF holds/outputs the sampled values. This condition continues until next rising edge of C. For the other combinations of (C, D), the FF holds the previous value. Note that (Ep, EpB)=(0, 0) never occurs because of specification of the SR-FF. The negative ET-FF operates in the similar way except for clock conditions.

Figure 4 shows state transition diagrams of the first stages of conventional ET-FFs. The difference of these two circuits is the clock transition direction only, and the other behaviors are the same each other. When the transitions of two bold solid lines or two bold dashed lines occur sequentially, both circuits sample the same value at the rising and falling edges. At this time, sampled data is proper data. For the other transitions, the circuit holds the previous value.

Now consider the relationship between the clock signal and the data signal. Considering the function of the DET-FF, there are four states for the relationship as shown in Fig. 5. In the proposed DET-FF, when the data signal at the rising edge is the same as the data signal at the falling edge (states (1) and (2) in Fig. 5), it is the proper signal. Then the DET-FF holds and outputs the signal. On the other hand, when the data signals at both edges are different each other (states (3) and (4)), the DET-FF recognizes that the noise signal comes to the FF input and the DET-FF must hold the previous value.

Table 1 summarizes the function of the DET-FF. States (1) and (2) are the cases of proper data, and then the DET-FF holds/outputs the value of D reached at the FF input. If the noise pulse reaches to the FF input (states (3) and (4)), the DET-FF holds the output value of the previous state. At this time, a warning signal plays the role of a flag to inform that the data signal at the rising edge is different from one at the falling edge. Its usage is explained later. For the other clock conditions (the last three rows in the table), the FF itself is in the hold state (state (Hold)), whose function is similar to conventional ET-FFs. Note that since the second stage (i.e., output state) of the conventional ET-FF is the SR-FF, (Ep, EpB)=(0, 0) and (En, EnB)=(1, 1) never occur.

Implementation example of a circuit satisfying the above function is shown in Figs. 6 and 7. The first stages of the conventional ET-FFs are the same as circuits shown in Fig. 3, which have the function to sample data at the clock edge. The second stage circuits are designed for satisfying the function of Table 1.

The DET-FF firstly samples data at the rising edge, and its value must be temporarily held until data is sampled at the following falling edge. In order to realize this function, the proposed DET-FF uses the two-input Muller C-element for the output stage of the rising edge part. The DET-FF must hold the previous value if the data value sampled by the falling edge is different from that of the temporary holding value (i.e., the data value sampled by the rising

edge). In addition, The FF must check whether those two values are the same or not comparing each other. In order to realize this function, the DET-FF uses the three-input Muller C-element for the output stage of the FF.
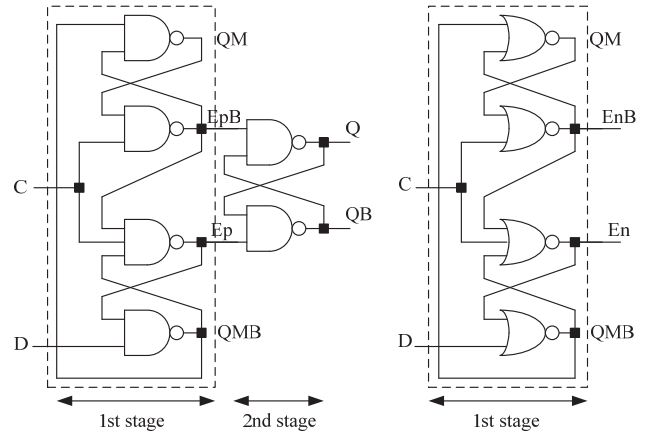

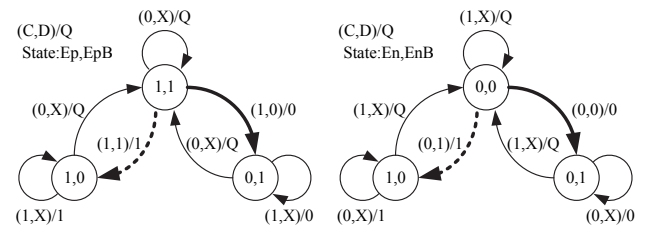Figure 3 Conventional edge triggered flip-flops.

Figure 4 State transition diagrams of first stages of conventional edge triggered flip-flops.
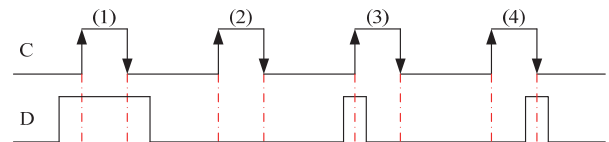

Figure 5 Relationship between clock and data signals.

Table 1 Function table of dual edge triggered flip-flop.

State	1st edge			2nd edge			Output		Warning
	C	D	Ep, EpB	C	D	En,EnB	Q	QB	
(1)	↑	1	1, 0	↓	1	1, 0	1	0	0
(2)	↑	0	0, 1	↓	0	0, 1	0	1	0
(3)	↑	1	1, 0	↓	0	0, 1	No change		1
(4)	↑	0	0, 1	↓	1	1, 0	No change		1
(Hold)	↓	X	1, 1	↑	X	0, 0	No change		0
(Hold)	0	X	1, 1	1	X	0, 0	No change		0
(Hold)	1	X	D_0, DB_0	0	X	D_0, DB_0	No change		0

Note: (Ep, EpB)=(0, 0) and (En, EnB)=(1, 1) do not exist.
D$_0$ and DB$_0$ denote previous values when C=1 (positive FF) or C=0 (negative FF).

The part enclosed with the dashed line of Fig. 6 temporarily holds the value sampled by the rising edge at the node Q1. The three-input C-element at the final stage has two functions. It firstly compares the temporarily

holding value with the value sampled by the following falling edge (i.e., a pair of (En, EnB)). Based on the comparison result of consistency/inconsistency of two values, the DET-FF outputs either the new sampled value or previous value.
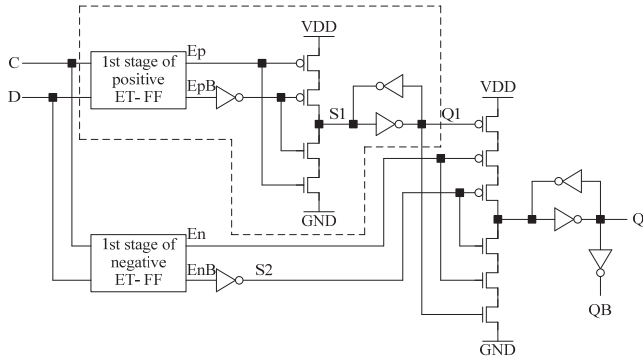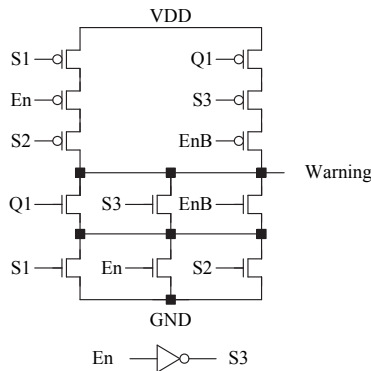

Figure 6 Dual edge triggered flip-flop.

Figure 7 Warning circuit of dual edge triggered flip-flop.

Until here, we assume the positive clock pulse. Exchanging (Ep, EpB) and (En, EnB), the circuit of Fig. 6 is applicable for the negative clock pulse.

A warning circuit of Fig. 7 informs us that there is the noise pulse (i.e., the value at the rising edge is different from one at the falling edge) producing the high level output. At this time, we know that the output of the DET-FF is the previous value because of blocking the noise pulse. This function is realized by the combination of Q1, En, EnB and their inversion signals. The warning circuit can function for both the positive clock pulse and the negative clock pulse.

5. Evaluation

The functions of Figs. 6 and 7 are verified by using 1.8 V 0.18-μm TSMC parameters. Figure 8 shows simulation results, where from the top, the figure shows the clock signal, the data signal, the output signals (solid line: DET-FF, dotted line: conventional positive ET-FF), and the warning output.

Data signal:
- (a) and (d): proper data signal
- (b) and (c): noise signal
- The data value is the logic 1 for intervals (a) and (d), and the logic 0 for the other intervals.

FF output signal:
- The DET-FF outputs the logic 1 for intervals (a1) and (d1) that correspond to intervals (a) and (d) of the logic 1 input, and the logic 0 for the other interval including noise pulses of (b) and (c). Thus the DET-FF can block noise pulses of (b) and (c).
- The conventional positive ET-FF outputs the logic 1 for the interval (b1) responding to the noise of (b) as well as intervals of (a) and (d) of proper signals. Thus, it malfunctions because of the noise pulse.

Warning output:
- The warning circuit outputs the warning signal for the intervals of (b2) and (c2) whenever noise pulses (i.e., (b) and (c)) appear on the data line. Thus, the circuit informs us that the noise pulse appears on the data line and it is blocked, and the DET-FF is holding the previous value.

From simulation results, we find the following observations.
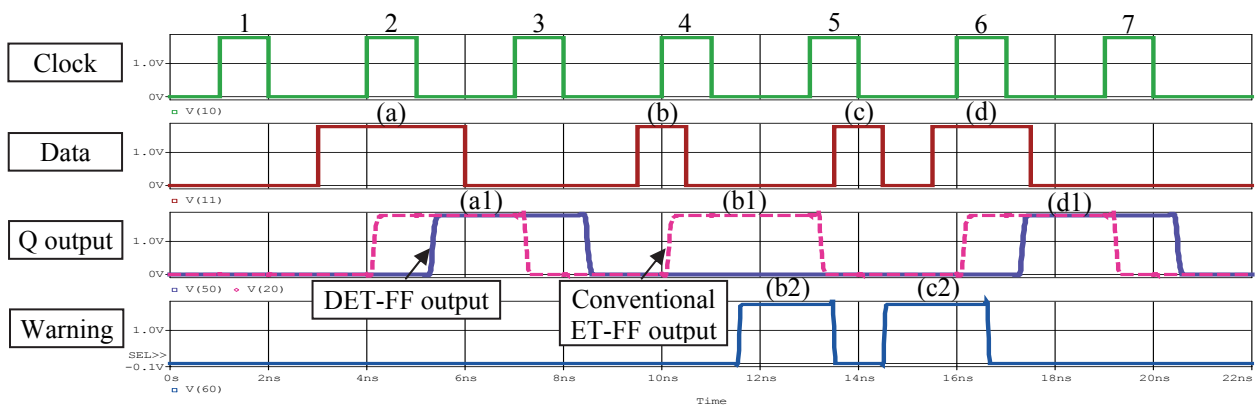

Figure 8 Simulation results of dual edge triggered flip-flop.

(1) DET-FF size: The number of transistors of the DET-FF (Figs. 6 and 7) is 74. If the same function of the DET-FF is realized by the combination of two conventional ET-FF, it requires a comparator, a multiplexer, a keeper, and a delay element. Then the number of transistors of its transistor level circuit is approximately 70 and the delay element. Transistor count of the proposed DET-FF is almost the same as the implementation by two conventional ET-FFs, but conventional one is needed the delay element. The DET-FF in this paper uses the first stage of the conventional ET-FF, however if we newly design this part, the DET-FF should become a smaller circuit, because the first stage circuit occupies 36 transistors among total transistors of the DET-FF (i.e., 49% of the total number of transistors).

(2) DET-FF performance: Table 2 summarizes AC characteristics of the DET-FF. Depending on a noise pulse type (positive or negative) and noise pulse generation timing, the DET-FF response differs. Values of [range] in the table mean the best value and the maximum value for each item. The noise width *tnw* that the DET-FF can block is determined by the clock pulse width *tw*. If *tw*=0.351 ns, the DET-FF can block surely the noise width between 0.231 ns and 0.351 ns (+*tsu*+*th*). Since the DET-FF uses two C-elements, propagation delay is relatively large. The minimum functional period *T* of the DET-FF alone is calculated as follows: *T*=*tw*+*tsu*+max(*th*, *tpQ*, *tpW*)= 1.121 ns. Then, maximum operating frequency is approximately 892 MHz

(3) Noise blocking ratio: The noise blocking ratio, NBR, within one clock period of the DET-FF is calculated by using Fig. 9. Let *a*=*tw*, *b*=*tnw*, here, *b*=αa (0<α<1), 0<*a*<2/*T* for simple equations. For case 1, the DET-FF can block the noise signal around edges:

$$(b/T)*2 = 2\alpha a/T. \qquad (1)$$

For cases 2 and 3, the noise signal occurring the other interval dose not influence FF function:

Table 2 AC characteristics.

| | | DET-FF | | Conventional FF | |
		max	[range]	positive	negative
minimum clock pulse width	tw [ns]	0.351		-	-
setup time	tsu [ns]	0.019	[-0.156, +0.019]	0.060	0.117
hold time	th [ns]	0.191	[0.022, 0.191]	0.292	0.200
propagation delay of Q	tpQ [ns]	0.493	[0.342, -0.493]	0.241	0.246
propagation delay of warning	tpW [ns]	0.751	[0.241, 0.751]	-	-
minimum noise width	tnw [ns]	0.231	[0.141, 0.231]	-	-
minimum noise amplitude	Vn [V]	1.007	[0.861, 1.007]	1.009	0.901
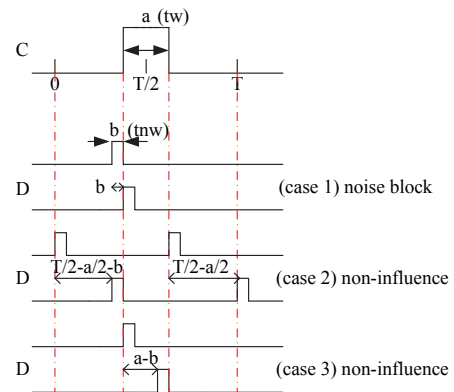
Figure 9 Noise blocking ratio.

$$((T-a-b)/T)+(a-b)/T=(T-2b)/T =(T-2\alpha a)/T. \qquad (2)$$

From equations of (1) and (2), NBR is calculated as:

$$NBR=(1)/(2)= 2\alpha a/(T-2\alpha a)=2b/(T-2b). \qquad (3)$$

From (3), we find that NBR depends on the width of the noise pulse (clock pulse) if the width of the clock pulse (noise pulse) is constant.

(4) DET-FF behavior (application to other error): We design the DET-FF as a noise aware technique. In addition, the proposed DET-FF can find timing violation of the data signal that results in extra delay. In the policy of DET-FF design, the data signal must arrive before the first edge of the dual-edge. Therefore,
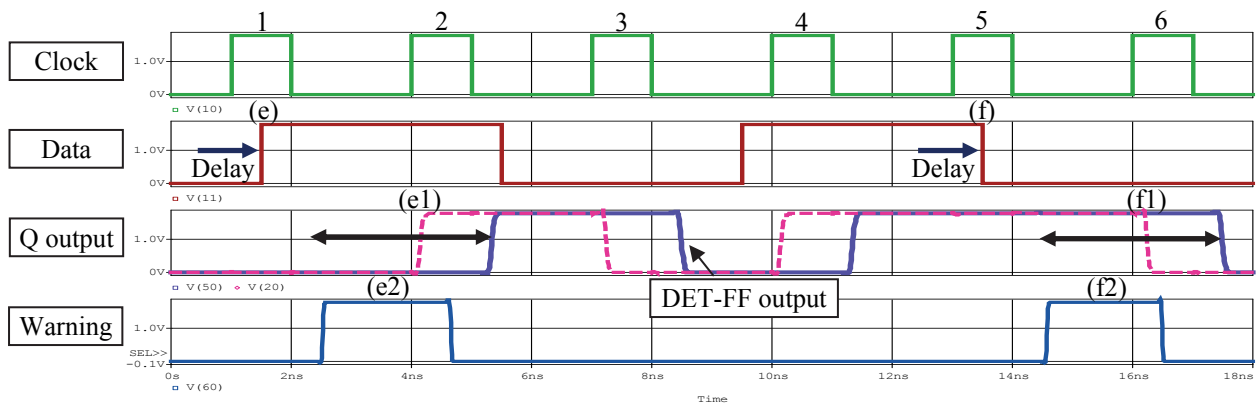
Figure 10 Example of timing violation of data signal.

if a signal change happens between two edges of the dual-edge, there is extra delay (e.g., delay fault) or timing violence by some reasons. In this case, since signal values between the rising edge and the falling edge are different, the DET-FF can find it. Figure 10 shows those simulation results. Signal transition to the logic 1 (0) is delayed at (e) ((f)), the warning flag is outputted at (e2) ((f2)), and we find there is timing violence in the data signal. For both cases (e) and (f), the DET-FF holds the previous value, however, for (e) ((f)), it seems that the DET-FF outputs the logic 0 (1) state as an extra output of just one clock period. However, this behavior is the nature of ET-FFs, not incorrect behavior.

6. Conclusions

This paper proposed the dual edge triggered flip-flop, DET-FF, which can block the noise pulse by using two edges of the clock signal. The DET-FF informs us that there is the noise signal on the data line by outputting the warning signal and the FF holds the previous value. We verified the DET-FF function by using circuit simulation. The DET-FF does not require any additional signal and delay element. So the application of the DET-FF to existing circuits is easy. In addition to noise pulse blocking, the DET-FF can apply to detection/correction of timing errors and delay faults that mean violence of timing constraint of FFs.

For implementing the DET-FF, this paper used the first stage circuit of the conventional ET-FF. For reducing the circuit size and improving performance, an implementation method must be improved. Besides, in order to show characteristics of the DET-FF, performance evaluation (e.g., speed, area, power, and application range, and etc.) compared with other similar methods is needed. This paper considered the edge triggered FF. We will apply the similar idea to the level sensitive (master-slave) FF. In addition, a noise generation/evaluation method is needed in future works.

Acknowledgement

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