

Delta Sigma Domain LDPC Decoder Based on Min-Sum Algorithm

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Abstract—Combination of interleaving and random error correction code is effective as a measure against burst error when power line is used for communication between ECUs in a car. However, since many ECUs are mounted in a car, miniaturization and cost reduction are required for reliable communication circuits. In this study, we construct an LDPC decoder circuit that performs error correction in the delta sigma domain based on the Min-Sum algorithm and attempts to downsize the circuit.

2. Delta Sigma Modulated Signal and Function Circuit

Circuits in the delta sigma domain are circuits that use a delta sigma modulated signal form for their input and output signals. In this study, the signals are first-order binary delta-sigma modulated.

2.1. First Order Delta Sigma Modulation

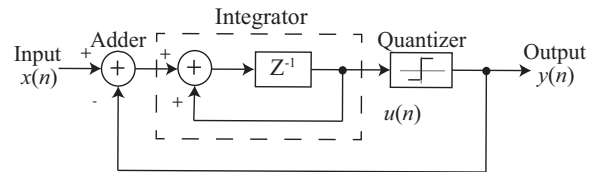


Figure 1: First order delta sigma modulator

1. Introduction

In recent years, computerization of automobile technology has advanced. Today, several tens to hundreds of computers called ECU (Electronic Control Unit) are mounted per car. The number of wires required for communication among a large number of ECUs is enormous, the use of power lines is being considered. However, since impulsive noises emitted by drive-train such as an engine and a motor are superimposed on a power line, a burst error occurs in the communication [1]. As a countermeasure for burst error, a combination of interleaving and random error correction coding is common. However, as mentioned above, since many ECUs are mounted in a car, downsizing and cost reduction of circuits for improving the reliability of communication are required.

The LDPC (Low Density Parity Check) code [2] is a long linear block code associated with a very sparse parity check matrix. By applying a decoding algorithm based on probability propagation [3], the LDPC not only achieves transmission capability approaching the Shannon limit but also has the advantage of decoding in linear time. Consequently, it is put to practical use as a code with high error correction capability.

Delta-sigma domain functional circuits operate on delta-sigma modulated signals and output signals in the same form [4][5]. The adder and absolute delta-sigma domain circuit used in this study are built simply and reduction of the scale of the LSI to which they are applied is expected. In this study, we aim to reduce the size of the LDPC decoder based on the Min-Sum algorithm by applying the delta-sigma domain circuits.

The first order delta-sigma modulator [6] is constructed as shown in figure 1. The locally averaged value of the output is forced to track the input by the integrator and the feedback loop, that is $\overline{y(n)} \approx x(n)$, and the signal band components of the quantization noise are swept out to the high frequency band.

The operation of the first-order delta-sigma modulator is expressed by the following equation:

$$u(n+1) = u(n) + x(n) - y(n) \quad (1)$$

$$Q(u(n)) = \begin{cases} 1 & \text{if } u(n) \geq 0 \\ -1 & \text{if } u(n) < 0 \end{cases} \quad (2)$$

$$y(n) = Q(u(n)) \in \{+1, -1\} \quad (3)$$

where n is the time index. The output $Q(u(n))$ of the quantizer is expressed by equation (2).

2.2. Function Circuit in Delta Sigma Domain

Delta-sigma domain circuits, an adder, a signum function, an absolute circuit, and a Min-Max circuit, are explained [4] [5].

The adder is constructed as shown in figure 2. The sorting circuit [7] in the adder outputs +1 (-1) at its center output terminal if the sum of their inputs is larger (smaller) than the given threshold value. The input sum and output sum of the sorting circuit are equal. Also, the output of the

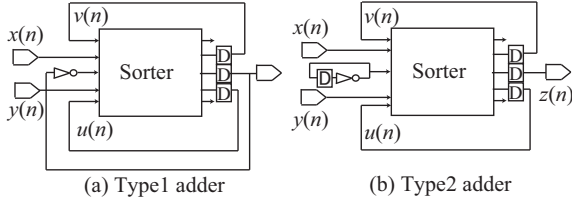


Figure 2: Adder circuit

sorting circuit is fed back through unit time delay (D). Assuming that the sum of the uppermost and the lower most outputs of the sorting circuit is 0, then Type1-adder and Type2-adder in 2 can be represented by the following equations (4) and (5) respectively:

$$\begin{aligned} u(n+1) + v(n+1) + z(n+1) \\ = u(n) + v(n) + x(n) + y(n) - z(n) \end{aligned} \quad (4)$$

$$\begin{aligned} u(n+1) + v(n+1) + z(n+1) \\ = u(n) + v(n) + x(n) + y(n) \pm 1 \end{aligned} \quad (5)$$

From equations (4), (5), $\overline{u(n+1)} \approx \overline{u(n)}$, and $\overline{v(n+1)} \approx \overline{v(n)}$, the outputs of the two types of the adders are given by the following equation:

$$\text{Type1 : } \quad \overline{z(n)} = \frac{\overline{x(n)} + \overline{y(n)}}{2} \quad (6)$$

$$\text{Type2 : } \quad \overline{z(n)} = \overline{x(n)} + \overline{y(n)} \quad (7)$$

The size of the adder circuit is about the same as the so-called full adder and one bit of the register. Therefore, the circuit scale can be greatly reduced as compared with conventional multi-bit adders.

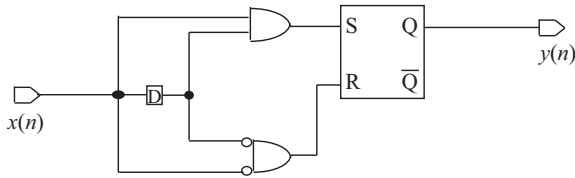


Figure 3: Signum function

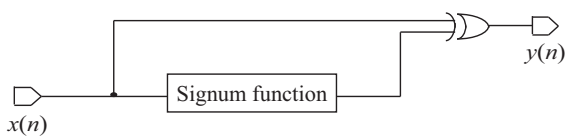


Figure 4: Absolute circuit

The signum function and the absolute circuit are constructed as shown in figures 3 and 4 respectively. The delta-sigma modulated signal has a characteristic that it does not

take -1 ($+1$) continuously when its local average is positive (negative). Therefore, by comparing the two consecutive bits of the delta-sigma modulated signal using one clock delay and SR flip-flop as shown in figure 3, its positive and negative can be judged. The absolute value of a delta-sigma modulated signal is obtained by the exclusive OR operation on the signal and the output of the signum function, as shown in figure 4.

The size of the absolute value circuit is about the same as that of one bit of 2's complement circuit. Therefore, the circuit scale can be greatly reduced as compared with the binary absolute value circuit.

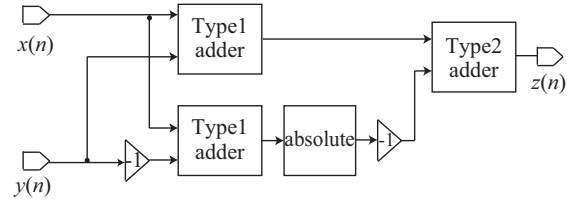


Figure 5: Minimum selector

As shown in the figure 5, the minimum selector can be constructed by using Type1 – adder, Type2 – adder, and an absolute value circuit. From the figure, the output can be represented by the following equation:

$$\begin{aligned} \overline{z(n)} &= \frac{\overline{x(n)} + \overline{y(n)}}{2} - \frac{|\overline{x(n)} - \overline{y(n)}|}{2} \\ &= \min(\overline{x(n)}, \overline{y(n)}) \end{aligned} \quad (8)$$

where $z(n)$ is the output and $x(n)$ and $y(n)$ are the two inputs.

3. Communication Method

3.1. Communication System

The model of the communication system using the LDPC code is shown in figure 6. In this study, the part that diffuses burst errors by interleaving is omitted. It is assumed that the generator matrix \mathbf{G} is obtained in advance from the parity check matrix \mathbf{H} . The code word (c_1, c_2, \dots, c_n) of the LDPC code is obtained by multiplying the k bit binary information vector (m_1, m_2, \dots, m_k) by the generator matrix \mathbf{G} . The codewords are sent to the channel through the modulator. The signal received through the channel is decoded by the decoder.

3.2. Binary input Gaussian noise channel

Each bit of the codeword is transformed to a bipolar signal x_i ($0 \rightarrow +1$, $1 \rightarrow -1$) and sent to an additive Gaussian white noise channel at time i . Then, at the received signal y_i is given by

$$y_i = x_i + n_i \quad (9)$$

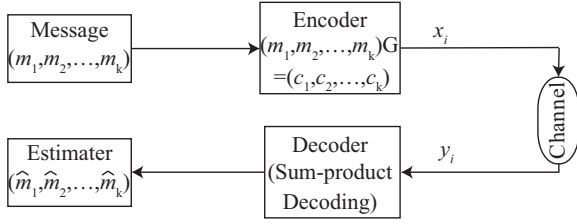


Figure 6: Communication system of LDPC code

4. LDPC Decoding

4.1. Tanner Graph and MAP Decoding Method

When the parity check matrix is expressed by the following equation, the transmission code estimation can be represented by a graph as shown in figure 7.

$$\mathbf{H} = \begin{pmatrix} 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 \end{pmatrix} \quad (10)$$

This is a bipartite graph called Tanner graph, which consists of variable nodes corresponding to each column of \mathbf{H} and check nodes corresponding to each row of \mathbf{H} . Since the nodes corresponding to 1 of \mathbf{H} are connected by edges, the number of branches of the Tanner graph is equal to the number of 1 of \mathbf{H} .

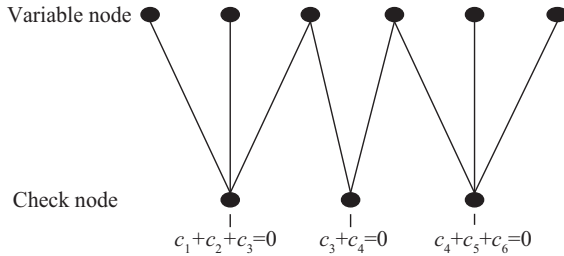


Figure 7: Example of LDPC code (Tanner graph representation)

The MAP(Maximum A Posteriori) decoding is a decoding method of estimating the most probable message from the received signal. More specifically, a posteriori probability $P(x_i = b|y)$, $b \in \{0, 1\}$, for the transmission codeword \mathbf{x} is calculated from the received codeword \mathbf{y} , and a symbol x_i that maximizes the posterior probability is taken as its estimate. The posterior probability is given by

$$P(x_k = b|y) = \sum_{\mathbf{x} \in \mathcal{C}, x_k = b} \prod_{i \in [1, n]} P(x_i) P(y_i | x_i) \quad (11)$$

where \mathcal{C} represents the entire set of codewords.

4.2. Min-Sum Algorithm

The Sum-Product decoding [2] is an approximate MAP decoding algorithm. In this study, we show Min-Sum decoding which performs Sum-Product decoding in the log-domain with simple approximate computation.

The binary $M \times N$ matrix \mathbf{H} is a check matrix of the LDPC code to be decoded. An m -th row and n -th column element H_{mn} of \mathbf{H} . The subsets $A(m)$, $B(n)$ of the set $[1, N]$ are defined as follows:

$$A(m) \triangleq \{n : H_{mn} = 1\} \quad (12)$$

$$B(n) \triangleq \{m : H_{mn} = 1\} \quad (13)$$

The flow of the algorithm is as follows:

Step 1 For all pairs (m, n) that satisfy $H_{mn} = 1$, let the logarithmic prior value ratio be $\beta_{mn} = y_n$ (y_n : received signal).

Step 2 The logarithmic external value ratio α_{mn} is updated using the following equation:

$$\alpha_{mn} = \left(\prod_{n' \in A(m) \setminus n} \text{sign}(u) \right) \min_{n' \in A(m) \setminus n} |u| \quad (14)$$

where u is $\lambda_{n'} + \beta_{mn'}$, and as n_i in equation (9) is Gaussian noise, the log-likelihood ratio is $\lambda_n = y_n$.

Step 3 Update β_{mn} with the following expression:

$$\beta_{mn} = \sum_{m' \in B(n) \setminus m} \alpha_{m'n} \quad (15)$$

Step 4 The temporary estimated word \hat{c}_n is obtained by using the following equation:

$$\hat{c}_n = \begin{cases} 0 & \text{if } \text{sign}(\lambda_n + \sum_{m' \in B(n)} \alpha_{m'n}) = 1 \\ 1 & \text{if } \text{sign}(\lambda_n + \sum_{m' \in B(n)} \alpha_{m'n}) = -1 \end{cases} \quad (16)$$

Step 5 It checks whether the temporary estimated word is a codeword. If $\hat{c}H^T = 0$ is satisfied, $(\hat{c}_1, \hat{c}_2, \dots, \hat{c}_N)$ is the estimated word and the algorithm is terminated. If not, return to Step 2.

5. LDPC Decoding Circuit in Delta Sigma Domain

A circuit that performs the Min-Sum decoding algorithm in the delta-sigma domain is constructed in this section. This circuit calculates the equation (14), (15), and (16) shown in 4.2 by the arithmetic units (adders, signum functions, absolute circuits, and Min-Max circuits) introduced in 2.2. It should be noted that the delta-sigma modulated signal form is a pulse waveform of -1 and 1 , and the local average value is limited to the range of $[-1, 1]$. Therefore, when obtaining the log-likelihood ratio λ_n from the received signal \mathbf{y} containing Gaussian noise, \mathbf{y} has to be scaled so that the averaged output of the arithmetic circuit is not saturated to ± 1 . In addition, the following equation is used as an approximate value L_n of the log posterior probability ratio as a measure to prevent the local average value from exceeding the range of $[-1, 1]$:

$$L_n = \frac{\lambda_n + \sum_{m' \in B(n)} \alpha_{m'n}}{p} \quad (17)$$

The denominator p is an integer obtained by adding 1 to the number of elements of $B(n)$.

6. Experimental Result

We carried out computer simulation of the operation of the decoding circuit described in section 5 with Simulink. We prepared $[1 \ 1 \ -1 \ 1 \ -1 \ -1]$ for the transmission signal and $[-0.1 \ 0.5 \ -0.8 \ 1.0 \ -0.7 \ 0.5]$ for the received signal as a result of the Gaussian noise being added (2 bits wrong if Hard Decision was done). This is applied to the delta-sigma domain decoder and a conventional real-valued decoder and their results are compared. The initial log liked ratio n is $[-0.07 \ 0.35 \ -0.56 \ 0.7 \ -0.49 \ 0.35]$. The parity check matrix handled is as follows:

$$H = \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 & 0 & 1 \end{bmatrix} \quad (18)$$

The local average value of the approximate value of the log posterior probability ratio computed in the delta sigma domain is shown in figure 8. Table 1 compares the average values with the results of real-valued decoding. It shows that the ratios are almost the same for all bits. The table validates that the sigma-delta domain decoding is successful.

7. Conclusions

In this study, LDPC decoding circuit was constructed using function circuit in the delta-sigma domain. It has been confirmed from the experiment results that the proposed decoding circuit in the delta sigma domain is accurately operated. As a feature of the delta sigma modulation, the quantization noise spectrum is large in the high frequency band. However, its influence was small, and the feedback loop was not unstable. The scale of the decoding circuit could be reduced because the row processing and the column processing can be executed only with the simple circuit described in 2.2. As a future work, we will attempt to execute decoding using the Min-Max algorithm in the delta sigma domain for the $GF(2^N)$ LDPC code, $N > 1$.

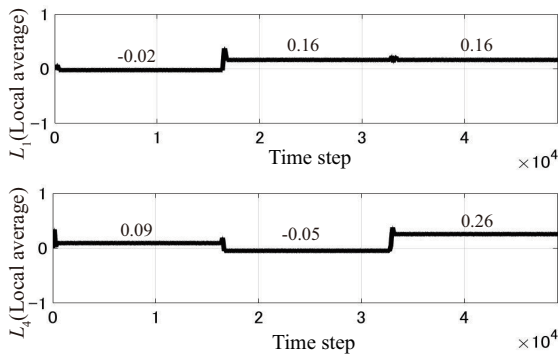


Figure 8: The values of L computed in the delta-sigma domain

Table 1: Comparison of log posterior probability ratios

bit	1	2	3	4	5	6
Real-valued	0.163	0.210	-0.163	0.256	-0.256	-0.070
$\Delta \Sigma$ domain	0.160	0.207	-0.164	0.258	-0.273	-0.070

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