ENHANCED VERSIONS OF THE DCSK SYSTEMS

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Abstract— Three different methods are proposed to improve the noise performance of *Differential Chaos Shift Keying* (DCSK) modulation scheme in this paper. DCSK is improved by modifying the structure of transmitted signal and the demodulation algorithm. It is shown how non-redundant error correction techniques can be applied to reduce the bit error rate (BER) considerably. The theoretical results derived for the BER are verified by simulations.

I. INTRODUCTION

In the past decade, many different modulation schemes have been proposed to exploit the potential benefits of chaotic signals in communications [1, 2, 3]. The most robust modulation scheme proposed in the literature is DCSK [4]. The basic idea of this modulation technique is that every information bit to be transmitted is represented by two chaotic sample functions. The first sample function serves as a reference while the second one carries the information. Bit "1" is sent by transmitting the reference chip twice in succession, while for bit "0", the reference chip is transmitted, followed by an inverted copy of the same signal. The two sample functions are correlated at the receiver; a positive correlation indicates that bit "1" has been received, while a negative value indicates bit "0".

In DCSK, half of the energy per bit is lost because the reference chip only provides the reference signal for the demodulator and does not carry any information. In order to reduce this loss, three different techniques are proposed which use modified versions of DCSK transmitter and receiver.

The loss is reduced in the simplest version of enhanced DCSK (DCSK/S) by transmitting $N > 1$ information-bearing chips using one reference chip as shown in Fig. 1 [5].

Depending on the information bit to be transmitted, the information-bearing chips are copies or inverted copies of the reference chip. In the original DCSK and DCSK/S receivers, the decision is made by determining the correlations between the information-bearing chips and the reference. However, note that additional information can be gained from the correlations between the information-bearing chips. In the most sophisticated versions of enhanced DCSK systems, the correlation between every pair of chips is evaluated at the receiver and this extra information is used to improve the noise performance.

Let $\tilde{r}_k(t) = \tilde{r}\left(t - \frac{k}{N+1}T\right)$, $k = 0, 1, \ldots, N$, denote the signal received in the kth time slot, where $\tilde{r}_0(t)$ is the reference and $\tilde{r}_k(t)$, $1 \le k \le N$, are the information-bearing chips. Let E_S denote the energy per chip. The correlation between the kth and lth chips is given by

$$z_{k,l} = \tilde{r}_k(t) \star \tilde{r}_l(t) = \int_0^{\frac{T}{N+1}} \tilde{r}_k(t)\tilde{r}_l(t)dt.$$

There are at least three ways to exploit the additional correlations in enhanced DCSK in order to improve its noise performance: enhanced DCSK with noise reduction by averaging (DCSK/AV) [6], enhanced DCSK with non-redundant "error correction" using the shortest path algorithm (DCSK/SP) and enhanced DCSK with non-redundant "error correction" using the spanning tree algorithm (DCSK/ST) [7].

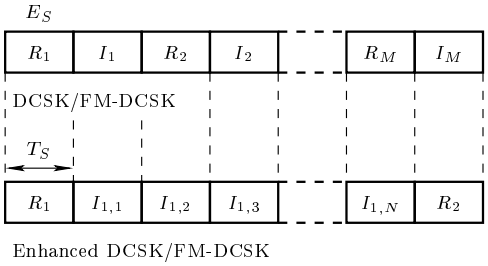

Figure 1: Typical time slots for the original DCSK systems (upper figure) and for the enhanced system (lower figure). One bit is transmitted on each time interval of $2T_S$ in the original system; N bits are transmitted in each time interval of $(N+1)T_S$ in the improved system.

II. ANALYSIS OF THE CORRELATIONS BETWEEN THE RECEIVED CHIPS

The redundancy carried by the enhanced DCSK signal can be exploited if a measure of goodness for each correlation can be found.

Let the probability of sending bits "1" and "0" be 0.5 and consider the correlation between the kth and lth chips. Figure 2 shows the histograms of $z_{k,l} = \tilde{r}_k(t) \star \tilde{r}_l(t)$. Note that in the region near the origin, the probability of making a wrong or correct decision is almost the same; the low absolute value of the correlation implies a high probability of a wrong decision.

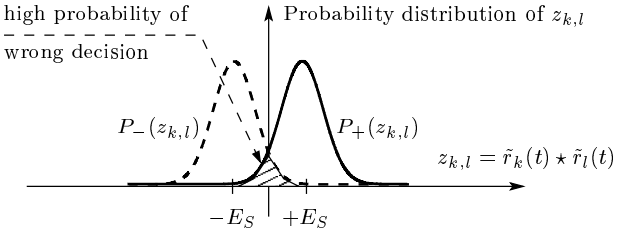

Figure 2: Probability distribution of the correlation between the kth and lth chips.

If the observation signal has a Gaussian distribution then can be fully characterized by the mean μ and the standard deviation σ of $P_+(z_{k,l})$ and $P_-(z_{k,l})$. Although the observation signal has a non-Gaussian distribution [8], for moderate noise level it can be approximated by a Gaussian one [9, 10, 11]. Hence, the probability distribution of $z_{k,l}$ is obtained as

$$P_\pm(z_{k,l}) = \frac{1}{\hat{\sigma}\sqrt{2\pi}} e^{(z_{k,l} \mp \mu)^2/(2\hat{\sigma}^2)} \tag{1}$$

where $\hat{\mu} = E_S$ while $\hat{\sigma}$ depends on the noise level, bit duration and the bandwidth of the signal.

From (1) we conclude that to minimize the probability of making a wrong decision at the receiver for $z_{k,l} \geq 0$ we have to assume that $s_k(t) = s_l(t)$ has been transmitted, while $s_k(t) = -s_l(t)$ should be assumed for $z_{k,l} < 0$. Hence, the probability of correct decisions is expressed by

$$\hat{P}_C(z_{k,l}) = \frac{\hat{P}_+}{\hat{P}_+ + \hat{P}_-} = \frac{1}{1 + e^{-2|z_{k,l}|\hat{\mu}/\hat{\sigma}^2}}. \tag{2}$$

III. NON-REDUNDANT ERROR CORRECTION IN THE EXTENDED DCSK SYSTEM

In this section we present three methods which improve further the noise performance of the enhanced DCSK system. These methods are referred later as "error correction" methods. However, please note that there is a significant difference between the error correction methods used in conventional digital communications systems and these methods.

At the receiver in our DCSK system, similarly to the conventional digital communications systems equipped with error correction, we have more information (observation signals), that is required to make the decisions for the transmitted information. Thus we are able to find an optimum decision strategy.

The main difference between our and the conventional digital communications systems equipped with error correction can be found at the transmitter part.

In conventional digital communications *extra bits are added* to each block of bits, these extra bits induce an algorithmic redundancy in the transmitted information which makes possible to use an error correction, at the receiver. As an example see the Viterbi algorithm [12]. In these systems we can design these additional bits in such a way that their Hamming distance [12] becomes maximum.

In the enhanced DCSK we *do not add any redundant bit* to the transmitted information, the extra information for the error correction is provided by the special structure of the enhanced DCSK signal. This is why our methods are called "non-redundant error corrections".

Our error correction do not exclude the application of standard error correction algorithms. In a built system, if required, the standard error correction blocks can be put on the top of our error corrections block and a further improvement in noise performance can be achieved.

A. NOISE REDUCTION BY AVERAGING IN THE IMPROVED DCSK SYSTEM

A further improvement in noise performance of the DCSK/S system can be achieved if we exploit the fact that every chaotic sample function is transmitted $(N+1)$ times. Every received chip is corrupted by noise. If the modulation is removed from the noisy received chips then the noise content of the reference signal can be reduced considerably by averaging the $(N+1)$ received noisy chips.

Let $\tilde{r}_l(t)$ denotes the received noisy chip in the lth time slot. To remove the modulation from $\tilde{r}_l(t)$, it has to be multiplied by

$$\text{sign}\left[\tilde{r}_0(t) \star \tilde{r}_l(t)\right],$$

i.e., by $\text{sign}(z_{0,l})$. Then an enhanced reference chip can be generated by averaging the $(N+1)$ chips

$$\hat{r}_0^*(t) = \frac{1}{N+1}\left\{\tilde{r}_0(t) + \sum_{l=1}^{N} \text{sign}(z_{0,l})\tilde{r}_l(t)\right\} \tag{3}$$

The noise reduction given by (3) works efficiently only if the modulation is removed correctly from the noisy incoming signal. If the estimation of the modulation determined by $\text{sign}(z_{0,l})$ is wrong then that term corrupts the efficiency of noise reduction instead of improving it.

To alleviate this problem, we introduce a scalar weighting factor $C_{0,l}$ which depends on the probability of correct decisions made by the $\text{sign}(\cdot)$ function. Thus, the enhanced reference chip is obtained as

$$\hat{r}_0(t) = \frac{1}{N+1}\left\{\tilde{r}_0(t) + \sum_{l=1}^{N} C_{0,l}\text{sign}(z_{0,l})\tilde{r}_l(t)\right\} \tag{4}$$

where $C_{0,l}$ has to be small if the probability of wrong decision is high.

An approximate analytical expression for the probability that a decision is correct is given by (2). Let us use this measure to obtain $C_{0,l}$.

First we estimate the mean $\hat{\mu}$ and the standard deviation $\hat{\sigma}$ of $z_{k,l}$. Having $\hat{\mu}$ and $\hat{\sigma}$, the probability of the correct sign of $z_{0,l}$ is computed by (2). Because the probability $\hat{P}_C(z_{0,l})$ covers the interval [0.5, 1.0] it has to be rescaled. Then the noise-free reference chip can be estimated by:

$$\hat{r}_0(t) = \frac{1}{N+1}\left\{\tilde{r}_0(t) + \sum_{l=1}^{N} 2[\hat{P}_C(z_{0,l}) - 0.5]\tilde{r}_l(t)\right\}. \tag{5}$$

Finally, this enhanced reference chip is used to perform the demodulation

$$\hat{b}_m = 0.5\text{sign}[\hat{r}_0(t) \star \tilde{r}_m(t)] + 0.5.$$

In order to determine the performance of the enhanced DCSK system with averaging, several simulations have been performed for different values of N. The results of these simulations are summarized in Sec. IV..

B. NON-REDUNDANT ERROR CORRECTION USING THE GRAPH THEORY

At least two enhanced DCSK with non-redundant error correction algorithms can be implemented which use combinational optimization techniques known from the graph theory. These are DCSK/SP [7] and DCSK/ST, employing the shortest path and the spanning tree algorithms, respectively.

In DCSK/SP and DCSK/ST, the correlations are calculated for each pair of chips and the probability of a wrong decision is minimized using the absolute values of these correlations. Since these error corrections differs only in the optimum search algorithm, for brevity, we discuss only DCSK/SP in detail. However the performance of DCSK/ST is included in Sec. IV for comparison.

The decision procedure is illustrated by the graph shown in Fig. 3, where the vertices of the graph represent all received chips, including the reference one, and the edges connecting the vertices represent the correlations between pairs of chips. It follows from the special structure of the enhanced DCSK signal that the decision for each bit can be made along any path in the graph which starts from k=0 and terminates at the desired chip. For example, if the decision has to be made for k=3 then, either of the following two decision paths can be used:

$$\text{sign}[\tilde{r}_{m,0}(t) \star \tilde{r}_{m,3}(t)] \quad \text{or}$$
$$\text{sign}[\tilde{r}_{m,0}(t) \star \tilde{r}_{m,4}(t)]\text{sign}[\tilde{r}_{m,4}(t) \star \tilde{r}_{m,3}(t)], \quad \ldots$$

where the decision is made in favor of bit "1" if these expressions are greater than one.

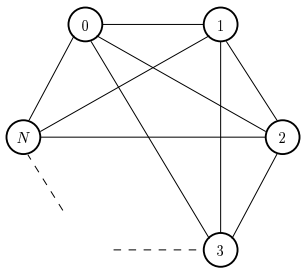

Figure 3: Graph showing all possible decision paths for an enhanced DCSK signal having one reference and N information-bearing chips. The vertices represent the received chips while the edges give the correlations between pairs of chips.

The *shortest path* algorithm [13] is used in DCSK/SP to select the decision path which offers the minimum probability of wrong decisions for the kth bits. In this approach, each edge of the graph shown in Fig. 3 is characterized by a weight, and each decision path is characterized by a cost which is the sum of these weights. The algorithm selects the path which has the minimum cost.

To minimize the BER, the weights associated with each edge must have a high value if the probability of a wrong decision is high, and a low one in the opposite case. Recall that (2) characterizes the probability of a correct decision, i.e., the weight for the edge connecting the kth and lth vertices can be defined as

$$w_{k,l} = -\log_2[\hat{P_C}(|\tilde{r}_k(t) \star \tilde{r}_l(t)|)]$$

Thus, a large weight is associated with each edge for which the probability of a wrong decision is high.

The steps of the enhanced DCSK technique are as follows:

- each reference chip is followed by N information-bearing chips, i.e., instead of individual bits, N-bit symbols are transmitted in one block;
- the correlations between all pairs of received chips are calculated;
- the weights associated with all edges are determined;
- using the shortest path algorithm, the decision path which offers the lowest probability of a wrong decision is selected for each of the N unknown bits;
- the decision is made for each bit using the edges of the corresponding shortest path.

IV. PERFORMANCE EVALUATION

An exact expression for the noise performance of original DCSK was given in [8]. In the simplest enhanced version of DCSK, denoted by DCSK/S, the energy per bit and the bit duration is reduced by sending N information bearing chips with one reference chip. Otherwise, there is no difference between DCSK and DCSK/S systems. Consequently, the noise performance of enhanced DCSK can be expressed by modifying equation (26) of [8]. Substituting the new values of bit duration $T_S(N+1)/N$ and energy per bit $E_S(N+1)/N$ we obtain:

$$\begin{aligned} BER = & \frac{1}{2^{2BT\frac{N}{N+1}}} \exp\left(-\frac{E_b N}{N_0(N+1)}\right) \\ & \times \sum_{i=0}^{2BT\frac{N}{N+1}-1} \frac{\left(\frac{E_b N}{N_0(N+1)}\right)^i}{i!} \\ & \times \sum_{j=i}^{2BT\frac{N}{N+1}-1} \frac{1}{2^j} \begin{pmatrix} j+2BT\frac{N}{N+1}-1 \\ j-i \end{pmatrix}. \end{aligned} \tag{6}$$

If N tends towards infinity (6) becomes exactly the noise performance of suboptimum non-coherent DPSK system. Note, that assuming $N = \infty$ is impractical, but it give us a performance bound for the DCSK/S system.

For a hypothetical case when N tends towards infinity the noise performance of DCSK/AV tends toward that of an ideal coherent antipodal CSK [1, 8, 14] modulation scheme where the identical chaos synchronization is achieved and maintained, i.e., the additional energy and time to transmit the reference becomes negligible and the reference signal becomes noise-free. This gives the performance bound of this system.

To compare the effectiveness of the different techniques, the noise performances of enhanced DCSK systems were

evaluated by computer simulation for the following system parameters: $2B$=17 MHz, $T = 2$ μs and N=4.

The noise performance of the DCSK/S, DCSK/AV, DCSK/ST and DCSK/SP is shown in Fig. 4. Recall that in DCSK/S one reference chip is used to transmit N information chips and no further processing is performed. In the other cases, the additional techniques described above are used in order to improve the noise performance of the system.

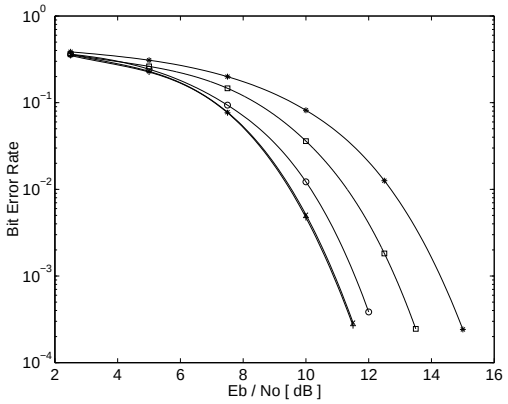

Figure 4: Noise performance of the the different enhanced DCSK systems. The curves for DCSK/SP, DCSK/ST, DCSK/AV and DCSK/S are represented by "+", "×", "○" and "□" marks, respectively. Note that the noise performance of DCSK/SP and DCSK/ST is almost the same. The noise performance of the original DCSK system (solid curve with "∗" marks) is shown for comparison.

The highest improvements in noise performance are achieved by applying the shortest path and the minimum cost spanning tree algorithms. Note that these two methods yield almost identical improvements in noise performance. An improvement of 3.4 dB can be achieved at BER=10^{-3}, as shown in Fig. 4.

The cost of higher noise performance and data rate is a more complex system configuration.

V. CONCLUSIONS

The paper showed how the noise performance of DCSK system can be improved considerably by changing the transmitter and receiver configurations. In the enhanced systems, in contrast with the standard DCSK system, instead of transmitting only one information-bearing signal after the reference signal, N bits are transmitted using the same reference. In the enhanced DCSK systems additional BER reduction is performed by averaging and non-redundant error correction techniques.

It was shown both by theoretical results and simulations that using the proposed techniques the data rate can be increased, the bit energy can be reduced and the noise performance of the DCSK transmission can be improved considerably.

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