Design and Analysis of Class DE–E DC/DC Converters with Any Output Q of The Inverter and Any Duty Ratio

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1. Introduction

Class DE–E dc/dc converter [1]–[3] is composed of class DE inverter [4] and class E rectifier [5]. Both class DE inverter and class E rectifier achieve high power conversion efficiency under high frequency (MHz order) operation because of class E switching conditions [6]. Therefore, class DE–E dc/dc also has ability to operate above 1 MHz with high power conversion efficiency.

The derivation of the waveform equations is a quite important problem of research on class DE–E converter. The waveform equations are useful to investigate the characteristics for a load variation, a input variation, a control [2], [3], and so on. The waveform equations of class DE–E converter are presented in [1] from approximate analysis. However, some conditions, i.e., high output Q of the inverter and 25% duty ratio, must be assumed in the analysis of [1]. In the previous researches, the analyses of the class DE–E dc/dc converters were always carried out before the converter was designed. That is because we needed the waveform equations of the converter for the design. Therefore, there is no method to derive the waveform equations of class DE–E dc/dc converters with any out put Q of the inverter and any duty ratio.

On the other hand, recently, the design method of class E inverter without using waveform equations was proposed [7]. This is the first design procedure which never need waveform equations for the design of class E inverter. Moreover, we can design class E inverter with any conditions with high accuracy by using this design procedure. If this design method can be applied to the design of class DE–E dc/dc converter, we can design the converter with any conditions before the derivations of waveform equations and may derive the waveform equations easily.

This paper presents a novel procedure of the derivation of the waveform equations for class DE–E dc/dc converter with any output Q of the inverter and any duty ratio. The main idea of this paper is the order of the 'analysis and design' is changed to 'design and analysis'. By using the design procedure based on [7], we can design class DE–E dc/dc converter with any conditions, namely, with any output Q of the inverter and any duty ratio. If the design values are known, the waveform equations can be derived easily by solving the circuit equations. Carrying out the circuit experiments, we show the validity of the design procedure and the waveform equations derived from proposed procedure.

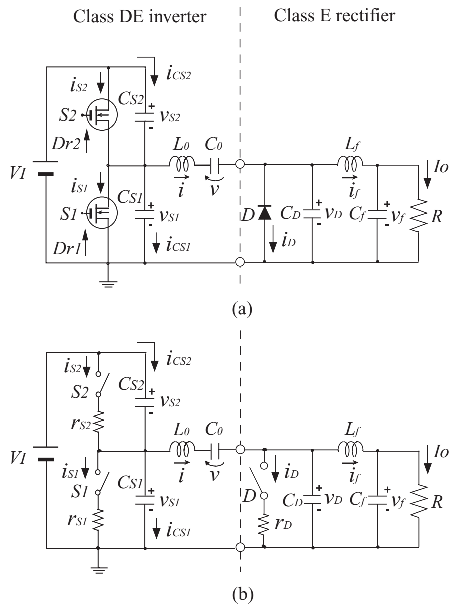

Figure 1: (a) Circuit topology of class DE–E dc/dc converter. (b) Equivalent circuit for proposed design procedure

2. Circuit description

Figure 1 (a) shows the circuit topology of Class DE–E dc/dc converter. Class DE–E dc/dc converter consists

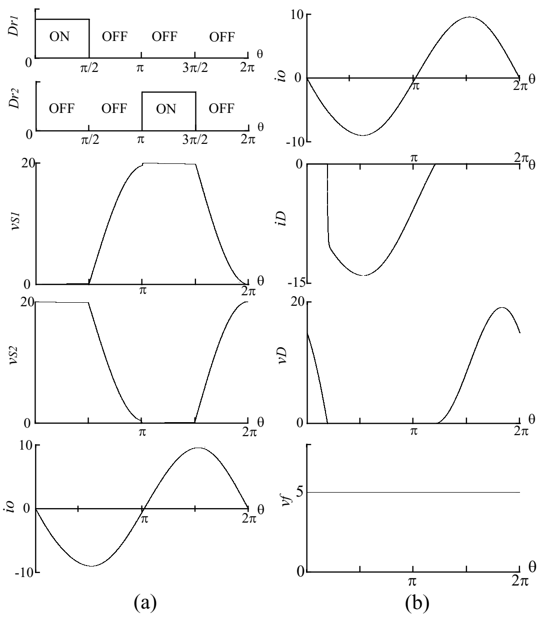

Figure 2: Nominal waveform of class DE–E dc/dc converter for $V_I = 20$V, $V_o = 5$V, $R = 10\Omega$, $K = 10$ and $D_S = 0.25$ from waveform equations. (a) The waveform of inverter part. (b) The waveform of rectifier part.

of Class DE inverter [4] and Class E rectifier [5]. The former is on the left side of the figure, and the latter is on the right side of it.

Class DE inverter consists of an input direct voltage source V_I, two switches S_1 and S_2, two capacitors C_{S1} and C_{S2} shunting the switches, and a series resonant circuit $L_0 - C_0$. The example of the waveforms of class DE inverter are shown in Fig. 2 (a), when switch on duty ratio is 25%. The switching losses are reduced to zero by the operating requirements of zero and zero slope of switch voltage at the turn on transition, called class E switching conditions [6]. On the other hand, class E rectifier consists of a diode D with a shunting capacitor C_D, a low-pass filter $L_f - C_f$, and load resistance R. In the rectifier, its input is ac current i supplied from the inverter and the output current I_o. At the diode turn-off transition, the capacitor current is zero. Therefore, the derivative of the diode voltage dv_D/dt is also zero as shown in Fig. 2 (b). This is also characteristic of Class E circuits. That reduces the switching losses and noises, and enables the rectifier to operate with high power conversion efficiency at high operating frequency.

3. Design and analysis procedure of class DE–E dc/dc converter

In this section, we present the design procedure of class DE–E dc/dc converter with any output Q of the inverter, any duty ratio and switch on resistance. This design procedure is based on the design procedure for class E amplifier without using waveform equations [7].

At first, the design given below is based on the following assumptions. These assumptions are, however, not always necessary.
1) The switching devices S_1, S_2 and D have zero switching times, infinite off resistance and on resistance r_{S1}, r_{S2} and r_D respectively.
2) All passive elements are ideal.
3) The shunt capacitance C_{S1}, C_{S2} and C_D include switch device capacitance.

Next, the following parameters of the circuit are defined.
1) $\omega_0 = 2\pi f_0 = 1/\sqrt{L_0 C_0}$: The resonant angular frequency.
2) $A = (f_0/f)^2 = (\omega_0/\omega)^2$: The ratio of the resonant frequency and the operating (switching) frequency.
3) $B = C_0/C_S = C_0/(C_{S1} + C_{S2})$: The ratio of the capacitance of a resonant capacitor to a shunt capacitor of the switch S.
4) $J = C_0/C_D$: The ratio of the capacitance of resonant capacitor to shunt capacitor of the diode D.
5) $K = \omega L_0/R$: The relationship of L_0 and C_0. This definition is similar to that of the loaded quality factor of the inverter.
6) D_S : The switch on duty ratio of the switch S_1 and S_2. D_S is defined in $0 < D_S < 0.5$.

By above assumptions, the equivalent circuit of this design procedure is shown in Fig. 1 (b). Compared with previous design [1], it is possible for this design procedure to consider any output Q of the inverter, any duty ratio, and switch on resistance. We consider the circuit operation in the interval $0 \leq \theta \leq 2\pi$, where $\theta = \omega t$ represents angular time. And the circuit equation are expressed as follows:

$$\begin{cases} \dfrac{dv_{S1}}{d\theta} = ABKR\left(\dfrac{V_I}{R_{S2}} - \left(\dfrac{1}{R_{S1}} + \dfrac{1}{R_{S2}}\right) v_{S1} - i\right) \\ \dfrac{di}{d\theta} = \dfrac{1}{KR}(v_S - v - v_D) \\ \dfrac{dv}{d\theta} = AKRi \\ \dfrac{dv_D}{d\theta} = AJKR\left(i - \dfrac{v_D}{R_D} - i_f\right) \\ \dfrac{di_f}{d\theta} = \dfrac{1}{2\pi f L_f}(v_D - v_f) \\ \dfrac{dv_f}{d\theta} = \dfrac{1}{2\pi f C_f}\left(i_f - \dfrac{v_f}{R}\right). \end{cases} \qquad (1)$$

In (1), R_{S1}, R_{S2} and R_D mean the resistance of the switch S_1, S_2 and the diode D, respectively. When we define that the switch S_1 turns on at $\theta = 0$, R_{S1} and R_D

are given as follows from Assumption 1.

$$R_{S1} = \begin{cases} r_{S1} & \text{for} \quad 0 \le \theta < 2\pi D_S. \\ \infty & \text{for} \quad 2\pi D_S \le \theta < 2\pi, \end{cases} \tag{2}$$

$$R_{S2} = \begin{cases} r_{S2} & \text{for} \quad \pi \le \theta < \pi + 2\pi D_S. \\ \infty & \text{for} \quad 0 \le \theta < \pi, \quad \pi + 2\pi D_S \le \theta < 2\pi, \end{cases} \tag{3}$$

$$R_D = \begin{cases} r_D & \text{for} \quad v_D \le 0 \\ \infty & \text{for} \quad v_D > 0. \end{cases} \tag{4}$$

Using above equations, we can design class DE–E dc/dc converter with any output Q of the inverter, any duty ratio, and switch on resistance. Class E switching conditions are given as

$$v_{S1}(2\pi) = 0, \tag{5}$$

$$\left.\frac{dv_{S1}(\theta)}{d\theta}\right|_{\theta=2\pi} = -ABKRi(2\pi) = 0. \tag{6}$$

Moreover, the output voltage V_o is given as

$$V_o = \frac{1}{2\pi}\int_0^{2\pi} v_f(\theta)\ d\theta. \tag{7}$$

In this paper, we set A, B, and J as design parameters and the other parameters are given as the design specifications. From (5) – (7) and transient conditions of the voltage and the current at $\theta = 2\pi$ and $\theta = 0$, we can derive the design parameters by following the design procedures in [7] and [8]. The benefits of the proposed design procedure are as follows.
1. It is unnecessary to derive the waveform equations in the design procedure. Moreover, the steps of the design except derivation of the circuit equations are carried out with aid of computer. Hence, we can design class DE–E dc/dc converter with any conditions accurately with a few works.
2. When the circuit equations are derived, we can design class DE–E dc/dc converter. This means that the design procedure deals with the various conditions, e.g., any output Q of the inverter, any duty ratio, switch on resistance, and so on.

By the way, the circuit equations (1) are linear functions because of Assumptions 1 and 2. When the values of circuit elements are unknown, we cannot solve (1) since the roots of the characteristic polynomial cannot be derived analytically or numerically. Using the design procedure based on [7], however, the values of circuit elements are known. Therefore, the rigorous solutions of (1) can be derived since the roots of the characteristic polynomial are given numerically. Moreover, the design values of the converter with any conditions are also given. As a result, we can get the waveform equations of class DE–E dc/dc converter with any output Q and duty ratio easily.

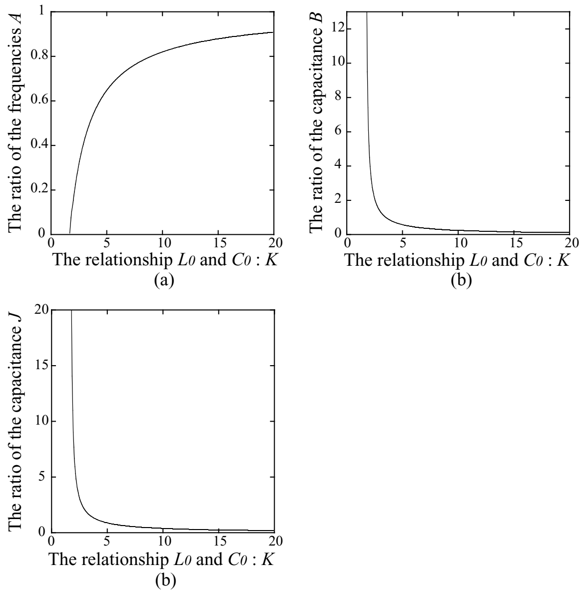

Figure 3: The design parameters as a function of K for $V_I = 20$V, $V_o = 5$V, $R = 10\Omega$ and $D_S = 0.25$. (a) The design curve of A. (b) The design curve of B. (c) The design curve of J.

4. Example of design and analysis

At first, the design specifications are given as follows : f=1.0MHz, $V_I = 20$V, $V_o = 5$V, $R = 10\Omega$, $r_{S1} = r_{S2} = 0.16\Omega$, and $r_D = 0.5\Omega$. In order to neglect the ac ripple on the dc output current, the low-pass filter of the rectifier $L_f - C_f$ is designed as $L_f = 270\mu$H and $C_f = 0.47\mu$F.

Figure 3 shows the design parameters as a function of K for $D_S = 0.25$. This figure shows the characteristic curves vary rapidly at about $K = 4$. That is because around $K = 4$ is the boundary between under-damped case and over-damped case of the inverter. Namely, in case of $K < 4$, the nonsinusoidal output of the inverter is generated. From Fig. 3, we can find the design values are greatly influenced by waveforms of the current through the resonant circuit. Figure 4 shows the design parameters as a function of D_S for $K = 10$. From this figure, there is a limit of D_S for this specification. In this specification, the maximum of D_S is 0.362. From Figs. 3 and 4,, it is confirmed that we can design class DE–E converter with any output Q of the inverter and any duty ratio.

Next, we carry out circuit experiments for $K = 10$ and $D_S = 0.25$. IRF530 MOSFETs are used as switch S_1 and S_2. Moreover, we use Schottky barrier diode 11DQ04 as a diode D. Following the design procedure based on [8], we derive the values of elements as $L_0 = 15.9\mu$H,

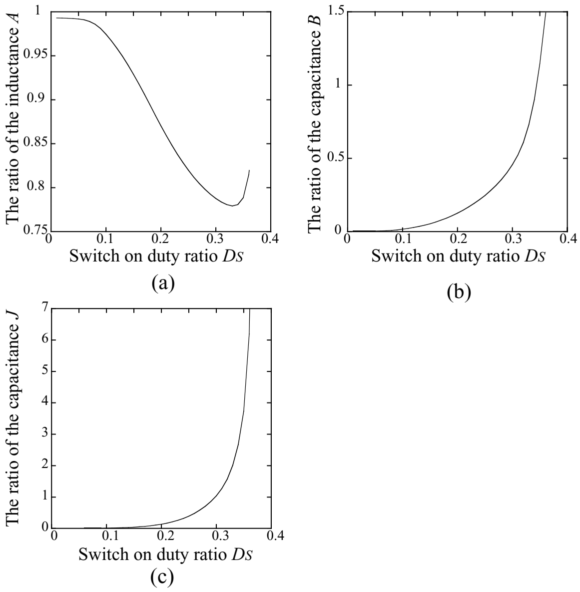

Figure 4: The design parameters as a function of K for $V_I = 20$V, $V_o = 5$V, $R = 10\Omega$, and $K = 10$. (a) The design curve of A. (b) The design curve of B. (c) The design curve of J.

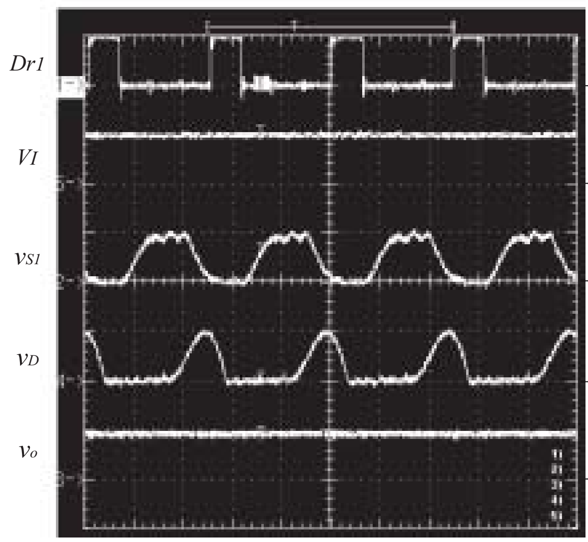

Figure 5: Experimental waveforms for $f = 1.0$MHz, $R = 10\Omega$, $V_I = 20$V, $V_o = 5.0$V, $K = 10$ and $D_S = 0.25$. Vertical: D_{r1} and v_f : 5V/div, V_I and v_{S1} : 20V/div, v_D : 10V/div. Horizontal : 400ns/div.

$C_{S1} = C_{S2} = 3.75\mu$F, and $C_D = 4.41\mu$F. Figure 5 depicts the experimental results. Moreover, we can derive waveform equations by solving (1). The waveform in Fig. 2 is drawn from the waveform equations. From Figs. 2 and 5, we show the validity of the design procedure and waveform equations.

5. Conclusion

This paper has presented a novel procedure of the derivation of the waveform equations for class DE–E dc/dc converter with any output Q of the inverter and any duty ratio. By using the design procedure based on [7], we can design class DE–E dc/dc converter with any conditions, namely, with any output Q of the inverter and any duty ratio. If the design values are known, the waveform equations can be derived easily by solving circuit equations. Finally, we make the source files for the program available on web-site : "http://www.icsd1.tj.chiba-u.ac.jp/sekiya/design/main.html".

Acknowledgments

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