An Integrated Double-Scroll Circuit Using Floating-Gate MOSFETs

Tetsuya Fujiwara[†], Yoshihiko Horio[†], and Kazuyuki Aihara[‡]

[†] Dept. of Electronic Engineering, Tokyo Denki University, Tokyo, 101-8457, Japan
[‡] Dept. of Mathematical Engineering, The University of Tokyo, Tokyo, 133-8656, Japan,
and CREST, JST., 332-0012, Kawaguchi, Japan

Abstract – This paper proposes an efficient technique for an integrated double-scroll circuit. The proposed circuit utilizes a high-Q MOS active inductor. Moreover, a negative conductance in the circuit is constituted with floating-gate MOSFETs. The characteristics of the double-scroll circuit can be altered by external control voltages, so that various chaotic dynamics can be easily obtained. The circuit is small, fast and compatible to a standard CMOS semiconductor process. The proposed circuit is designed and laid out with MOSIS TSMC 0.35 μm process. HSPICE circuit simulation results with extracted data from the layout are shown.

1 Introduction

Electric circuits with chaotic behavior can be found in many applications such as chaos communications [1], chaos encryption [2], optimization [3] and neural networks [4]. The double-scroll circuit (Chua's circuit) [5] is simple, versatile, and has been well investigated. Several techniques have been proposed to integrated the circuit [6, 7, 8]. However, those circuits occupy large die area and can operate only in low frequency.

This paper proposes a technique for a small and fast double-scroll integrated circuit. The passive inductor in the original circuit is replaced by a high-Q active inductor circuit [9]. Moreover, the fifth-order piece-wise linear negative conductance in the original circuit is realized with a combination of the Λ-type and V-type nonlinear resistor circuits [10] composed of floating-gate MOSFETs [11]. The V–I characteristics of the conductance can be altered by external control voltages. Therefore, various chaotic dynamics can be obtained. The proposed circuit is simple and compatible to a standard CMOS semiconductor process. Moreover, it occupies small area and operates at high-frequency. The proposed double-scroll circuit is designed and laid out with MOSIS TSMC 0.35 μm CMOS process.

In section 2, the double-scroll circuit is proposed, and the operation of the circuit is explained. In section 3, a prototype chip for the proposed circuit is shown with a layout. Finally in section 4, HSPICE simuration results using the data extracted from the layout are shown.

2 The Double-Scroll Circuit with Floating-gate MOSFETs

Figure 1(a) shows the original double-scroll circuit (Chua's circuit), which consists of two capacitors, C_1 and C_2, an inductor, L, a resistor, R, and a negative conductance, G_n. In contrast, Fig. 1(b) proposes a novel all MOS double-scroll circuit.

The negative conductance, G_n, in Fig. 1(a) is replaced by an N-type nonlinear conductance circuit using floating-gate MOSFETs [11]. With this circuit, 3rd to 7th order piece-wise linear conductance can be realized. Moreover, the slope of each piece-wise linear section and the positions of breakpoints can be adjusted externally.

The passive inductor in Fig. 1(a) is replaced by a high-Q active inductor [9] in Fig. 1(b). The active inductor has 2-stage RC phase-shift circuit. The conductance of the active inductor becomes zero or even negative by controlling the MOSFET resistor values in the phase-shift circuit with the external voltages.

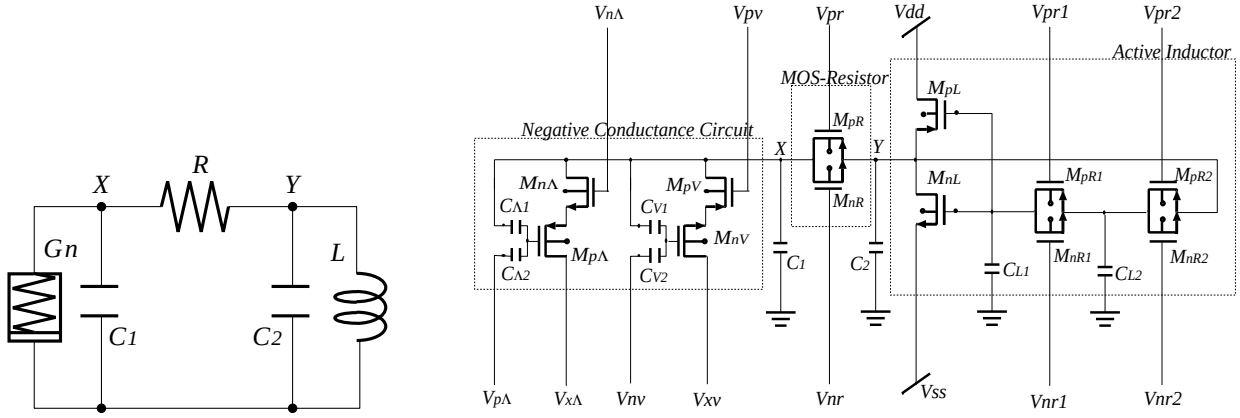
Resistor, R, in Fig. 1(a) is also replaced by a MOSFET resistor which is made up of a parallel connection of a P-MOSFET and an N-MOSFET in order to handle a wide voltage swing.

In the proposed circuit, the characteristic of the nonlinear conductance circuit, the active inductor, and MOSFET resistor can be changed separately. Therefore, various chaotic dynamics can be obtained from the circuit.

3 IC Implimentation

The proposed circuit in Fig. 1(b) can be integrated with standard CMOS semiconductor process. The layout of the prototype chip using MOSIS TSMC 0.35 μm CMOS process is shown Fig. 2. The power supply voltages of the chip are $V_{ss} = -1.65$ V and $V_{dd} = 1.65$ V.

In addition to the proposed double-scroll circuit, the N-type nonlinear resistor circuit, the active inductor, two capacitors (C_1 and C_2), the MOSFET resistor (M_{pR} and M_{nR}) and the phase-shift circuit in the active inductor (C_{L1}, C_{L2}, M_{pR1}, M_{nR1}, M_{pR2} and M_{nR2}) are individually intergrated for test purpose.



(a) (b)

Figure 1: The double-scroll circuit. (a) The original circuit, and (b) the proposed circuit. The bulk terminals of all N-MOSFETs and P-MOSFETs are connected to V_{ss} and V_{dd}, respectively.

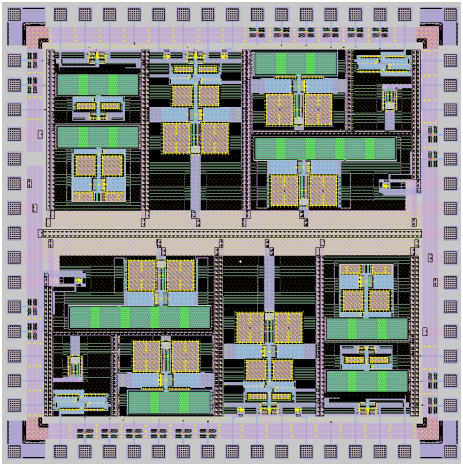


Figure 2: The layout of the prototype chip.

4 HSPICE Simulation Results

In this section, the HSPICE simurlation results using the circuit extracted from the layout in Fig. 2 are shown. The circuit parameters are summarized in Table 1.

Fig. 3 shows phase portraits in the V_x–V_y plane, where V_x and V_y are voltages of nodes X and Y in Fig. 1(b), respectively. These phase portraits are obtained by changing the control voltages $V_{n\Lambda}$, $V_{p\Lambda}$, V_{nV} and V_{pV}, while other voltages are fixed as $V_{x\Lambda} = V_{pR} = V_{prR} = V_{pR2} = -1.65$ V and $V_{xV} = V_{nR} = V_{nR1} = V_{nR2} = 1.65$ V. This parameter setting realizes the priode doubling route to chaos.

When the control voltages of the negative conductance circuit are set as $V_{n\Lambda} = 1.27$ V, $V_{p\Lambda} = -3.88$ V $V_{nV} = -1.52$ V, $V_{pV} = 3.73$ V, the double-scroll attractor shown in Fig. 3(d) is obtained. The V–I characteristics of the negative conductance, the admittance chart of the active inductor, and the time waveforms of V_x and V_y under this condition are shown in Figs. 4(a), (b) and (c), respectively. From Fig. 4(b), the real part of the admittance turns zero at about 7 MHz. Therefore, the fundamental frequency in Fig. 4(c) is around 7 MHz.

Figure 5 shows the results with different parameter settings shown in Table 2.

Table 1: The circuit prameters for HSPICE simulations.

Parameters in Fig. 1(b)	size
$(W/L)_{M_{n\Lambda}}, (W/L)_{M_{nV}}$	(18 μm/0.6 μm)
$(W/L)_{M_{p\Lambda}}, (W/L)_{M_{pV}}$	(54 μm/0.6 μm)
$(W/L)_{M_{nL}}$	(30 μm/0.6 μm)
$(W/L)_{M_{pL}}$	(80 μm/0.6 μm)
$(W/L)_{M_{nR1}}, (W/L)_{M_{nR2}}$	(1.8 μm/0.6 μm)
$(W/L)_{M_{pR1}}, (W/L)_{M_{pR2}}$	(3.6 μm/0.6 μm)
$(W/L)_{M_{nR}}$	(2 μm/1 μm)
$(W/L)_{M_{pR}}$	(6 μm/1 μm)
C_1	1.6 pF
C_2	10 pF
C_{L1}	4 pF
C_{L2}	16 pF
$C_{\Lambda 1}, C_{\Lambda 2}, C_{V1}, C_{V2}$	0.3 pF

5 Conclusions

An implementation technique of a small and fast double-scroll integrated circuit has been proposed. The characteristics of the proposed circuit can be changed by the external voltages. Therefore, various chaotic dynamics can be realized.

A prototype chip of the circuit has been designed and laid out using MOSIS TSMC 0.35 μm CMOS process. Various chaos dynamics have been observed through HSPICE simulations using the circuit data extracted from the layout of the chip. The prototype chip is currently under fabrication.

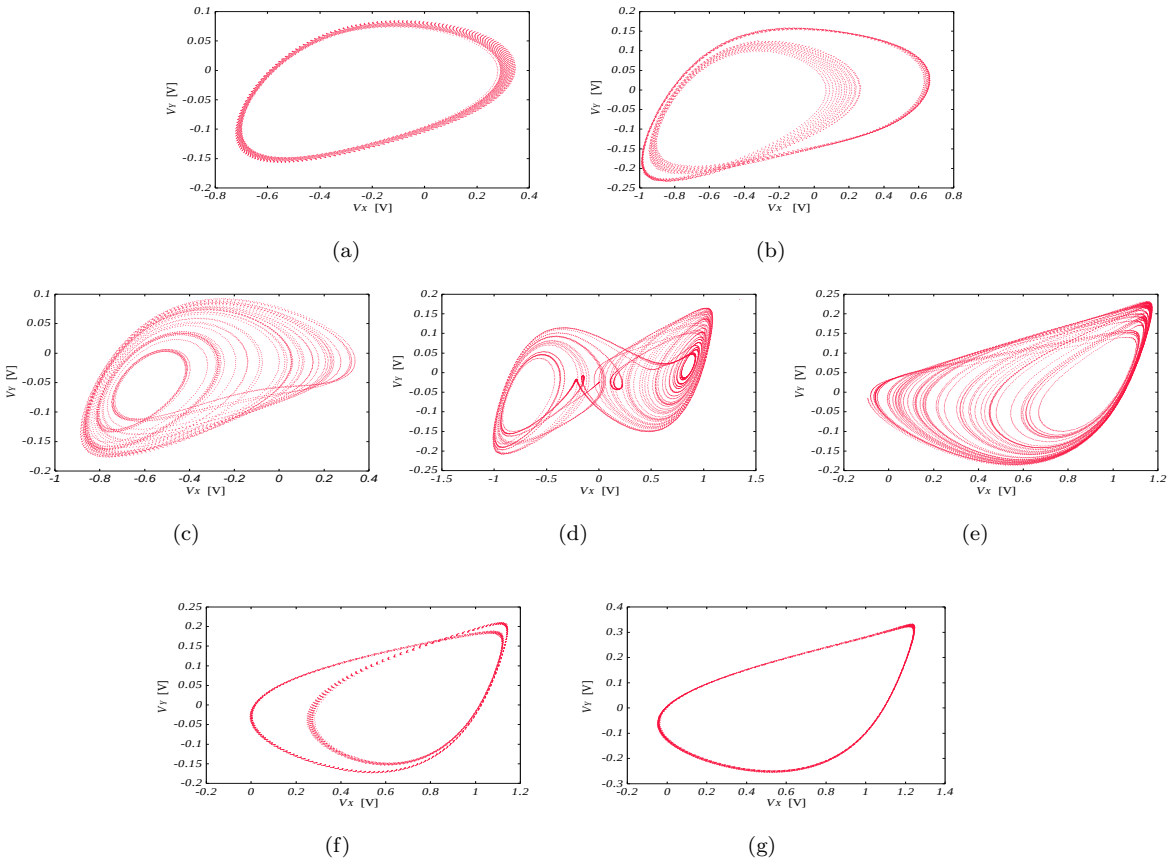


Figure 3: Phase portraits in the V_x–V_y plane (HSPICE simulation results). The control voltages $V_{n\Lambda}$, $V_{p\Lambda}$, V_{nV}, and V_{pV} are changed. (a) $V_{p\Lambda} = -3.88$ V, $V_{n\Lambda} = 1.21$ V, $V_{pV} = -1.46$ V, $V_{nV} = 3.73$ V, (b) $V_{p\Lambda} = -3.87$ V, $V_{n\Lambda} = 1.24$ V, $V_{pV} = -1.48$ V, $V_{nV} = 3.73$ V, (c) $V_{p\Lambda} = -3.86$ V, $V_{n\Lambda} = 1.27$ V, $V_{pV} = -1.52$ V, $V_{nV} = 3.73$ V, (d) $V_{p\Lambda} = -3.88$ V, $V_{n\Lambda} = 1.27$ V, $V_{pV} = -1.52$ V, $V_{nV} = 3.73$ V, (e) $V_{p\Lambda} = -3.87$ V, $V_{n\Lambda} = 1.32$ V, $V_{pV} = -1.55$ V, $V_{nV} = 3.76$ V, (f) $V_{p\Lambda} = -3.87$ V, $V_{n\Lambda} = 1.24$ V, $V_{pV} = -1.49$ V, $V_{nV} = 3.73$ V, and (g) $V_{p\Lambda} = -3.87$ V, $V_{n\Lambda} = 1.32$ V, $V_{pV} = -1.55$ V, $V_{nV} = 3.82$ V.

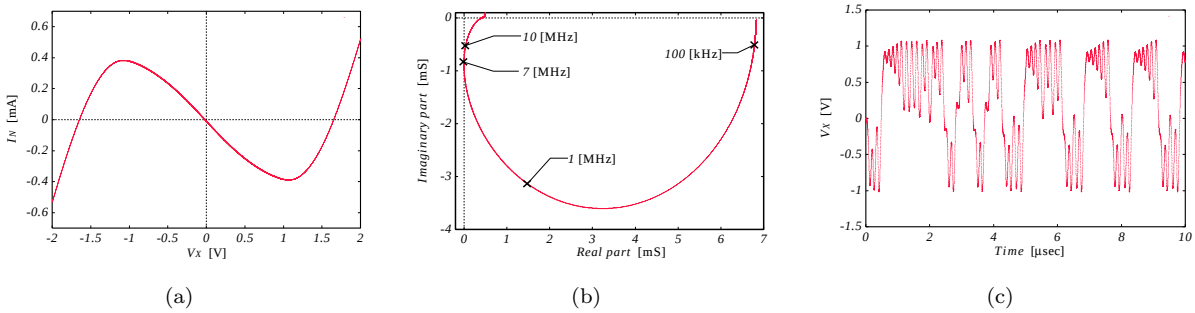


Figure 4: HSPICE simulation results. (a) The admittance chart of the active inductor, (b) the V–I characteristic of nonlinear circuit, and (c) the time waveform of V_x, for the attractor shown in Fig. 3(d).

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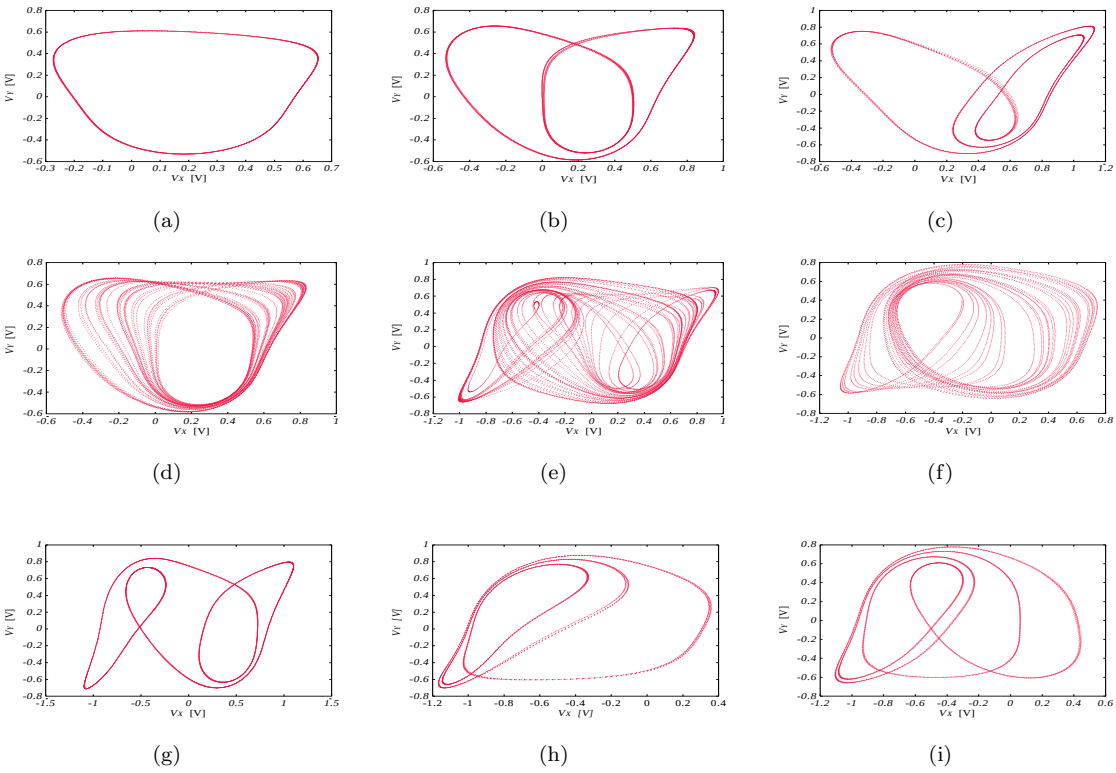

Figure 5: Examples of phase portraits in the V_x–V_y plane (HSPICE simulation results). The circuit parameters are given in Table 2.

Table 2: Circuit parameters of Fig. 1(b) for simulation results in Fig. 5.

	Phase portrait in Fig. 5								
Voltages in Fig. 1(b)	(a)	(b)	(c)	(d)	(e)	(f)	(g)	(h)	(i)
$V_{p\Lambda}$ [V]	-3.4	-3.55	-3.55	-3.5	-3.55	-3.45	-3.55	-3.55	-3.55
$V_{n\Lambda}$ [V]	0.85	0.85	0.92	0.85	0.88	0.95	0.92	0.92	0.92
$V_{x\Lambda}$ [V]	1.35	-1.35	-1.35	-1.35	-1.35	-1.65	-1.35	-1.65	-1.65
V_{pV} [V]	-1.05	-1.05	-1.13	-1.05	-1.08	-1.15	-1.12	-1.12	-1.12
V_{nV} [V]	3.3	3.45	3.42	3.4	3.42	3.27	3.42	3.42	3.42
V_{xV} [V]	1.35	1.35	1.35	1.35	1.35	1.65	1.35	1.63	1.65
V_{pR1}, V_{pR2} [V]	-1.18	-1.18	-1.18	-1.18	-1.18	-1.15	-1.21	-1	-1.25
V_{nR1}, V_{nR2} [V]	1.15	1.15	1.15	1.15	1.15	1.15	1.21	1.7	1.25
V_{pR} [V]	-0.8	-0.8	-0.8	-0.8	-0.8	-0.8	-0.8	0.79	0.8
V_{nR} [V]	0.8	0.8	0.8	0.8	0.8	0.8	0.8	-0.79	-0.8

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