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Multiple-input Maximum and Minimum Circuits Based on CCII

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Abstract

The multiple-input maximum (Max) and minimum (Min) circuits based on the second-generation current conveyor (CCII) are described. The simple configuration for n-input signals consist of (n+2) CCIIs, (2n) diodes and (n+1) resistors. The proposed scheme achieves a high accuracy and low crossover transition delay times. Finally, PSPICE simulation results demonstrating the circuit performance are also included.

1. Introduction

Multiple-input Max and Min circuits are basic building blocks in many advanced computational systems, such as image processing and fuzzy logic control [1]-[5]. Recently, the second generation current conveyor (CCII) has become very popular because of its high performance coupled with functional versatility [6]. CCII has been demonstrated, found it can be used to implement a 2-input Max/Min circuits for fuzzy logic controller [2]. Theoretically, the 2-input Max/Min circuit in binary tree structure is used to implement the multiple-input Max/Min Circuits. However, it still have errors and low operation speed [4]. Therefore, this paper shows the design of the multiple-input Max and Min circuits, which consist of the CCIIs, resistors and diodes.

2. Circuit description

2.1 Definition of the Ideal CCII

In figure 1 shows the circuit symbol of a CCII, which is the three port networks defined by the matrix relationship that exists between voltages and currents of its input-output ports:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad (1)$$

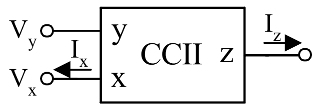

Figure 1. Circuit symbol of a CCII

In this expression, the cases $I_z=+I_x$ and $I_z=-I_x$ will be referred to the positive current conveyor (CCII+) and the negative current conveyor (CCII-), respectively. The input impedance for the ideal CCII are defined as infinite on port y and null on port x. The port z, is equivalent to a current generator, which possesses in consequence an infinite out put impedance. The positive CCII-based Max and Min circuits are presented in the following section.

2.2 The multiple-input Max circuit

The proposed multiple-input maximum (Max) circuit based on CCII is shown in figure 2. Assuming that all of the CCIIs are the ideal positive CCII[6]. The operation of the circuit can be explained as follow. The each of port y of $CCII_1$ to $CCII_n$ are employed as the input port for the signal voltage V_{in1} to V_{inn}, respectively. The $CCII_{B2}$ is the output voltage feedback buffer, which provide the bias voltage, V_{out}, for the D_{21} to D_{2n} diodes. The $CCII_{B1}$ is the feedback buffer, which coppy the output voltage to compare with the all of input voltage. If $V_{inj}>V_{out}$, then the current of, I_{zj}, $I_{zj}=I_{xj}=(V_{inj}-V_{out})/R_c$ will flow through the D_{1j} diode. If $V_{inj}<V_{out}$, then more current, are not flows through the D_{1j} diode, but there is the current, I_{zj}, $I_{zj}=I_{xj}=(V_{out}-V_{inj})/R_c$ will flow through the D_{2j} diode. Therefore, there is only transfer characteristic of the current with flows through the D_{1j} diode. I_{d1j} current is defined is

$$I_{d1j} = \begin{cases} (V_{inj} - V_{out})/R_i & for\ V_{inj} > V_{out} \\ 0 & for\ V_{inj} \le V_{out} \end{cases} \quad (2)$$

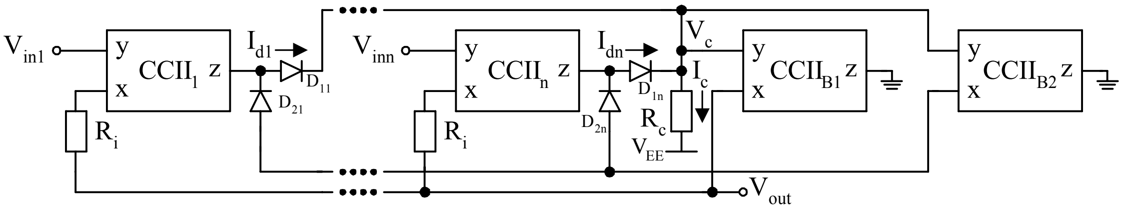

Figure 2. The proposed multiple-input Max circuit

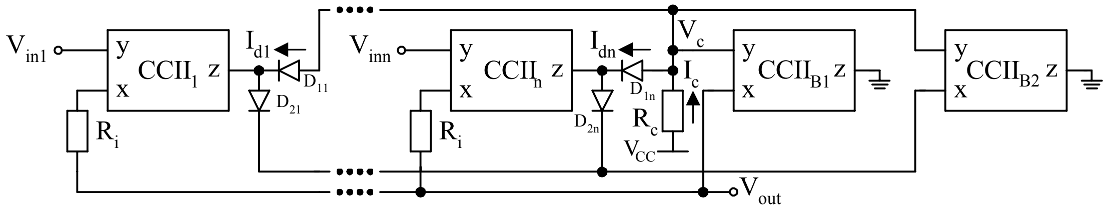

Figure 3. The proposed multiple-input Min circuit

, which

$$V_c = V_{EE} + R_c \sum_{j=1}^{n} I_{d1j} = V_{EE} + R_c I_c \qquad (3)$$

where V_{EE} is the negative-power supply voltage.

From equation (3), V_c is used as the voltage source for this circuit. Suppose that there is only one maximum input voltage of V_{in1} to V_{inj} and the out put voltage, V_{out}, is equal to V_c, so

$$V_{out} = \frac{R_c}{R_i + R_c} \max(V_{in1}, V_{in2}, \ldots, V_{inn}) + \frac{R_i}{R_i + R_c} V_{EE} \qquad (4)$$

where max(V_{in1}, V_{in2}, ….., V_{inn}) is the maximum input voltage of V_{in1} to V_{inn}, respectively. Let, R_c>>R_i then the output voltage, V_{out}, becomes to

$$V_{out} = \max(V_{in1}, V_{in2}, \ldots, V_{inn}) \qquad (5)$$

2.3 The multiple-input Min circuit

Figure 2 shows the proposed multiple-input minimum (Min) circuit. This modification is similar to the Max circuit, except for inverting-directional diode and positive supply. Similarly to the Max circuit, there is only transfer characteristic of the current flows through the D_{1j} diode, which are defined as

$$I_{d1j} = \begin{cases} (V_{out} - V_{inj})/R_i & for\, V_{inj} < V_{out} \\ 0 & for\, V_{inj} \geq V_{out} \end{cases} \qquad (6)$$

and

$$V_c = V_{CC} - R_c \sum_{j=1}^{n} I_{d1j} = V_{CC} - R_c I_c \qquad (7)$$

where V_{CC} is the positive-power supply voltage.

Figure (7), V_c is used as the voltage source for this circuit. Suppose that there is only one minimum input voltage of V_{in1} to V_{inn} and the out put voltage, V_{out}, is equal to V_c, so

$$V_{out} = \frac{R_c}{R_i + R_c} \min(V_{in1}, V_{in2}, \ldots, V_{inn}) + \frac{R_i}{R_i + R_c} V_{EE} \qquad (8)$$

where min(V_{in1}, V_{in2}, ….., V_{inn}) is the minimum input voltage of V_{in1} to V_{inn}, respectively. Similar to the Max circuit when R_c>>R_i, then the output voltage, V_{out}, becomes to

$$V_{out} = \min(V_{in1}, V_{in2}, \ldots, V_{inn}) \qquad (9)$$

3. Simulation results

To verify the performance of the proposed circuit technique, the circuit in figure 2 and 3 has been simulated by the PSPICE analogue simulation program.

The simulation, use the D1N4148 diode as parameter, 2N3906 and 2N3904 as the pnp and npn transistors, respectively. The current conveyor is taken from reference [7]. In all cases the bias current of all CCII were set to 0.5mA, the supply voltages were $V_{CC}=-V_{EE}=10V$. The values of the components are $R_i=100\Omega$ and $R_c=100k\Omega$. Figure 4 and 5, shows the simulated transient response for three input voltages of Max circuit and Min circuit, respectively. Figure 6 and 7, shows the simulated transient response for five input voltages of Max circuit and Min circuit, respectively. The obtained crossover transition time delays lower than 50ns. The output error of the full-scale value (2V) are ~2.5% (~50mV).

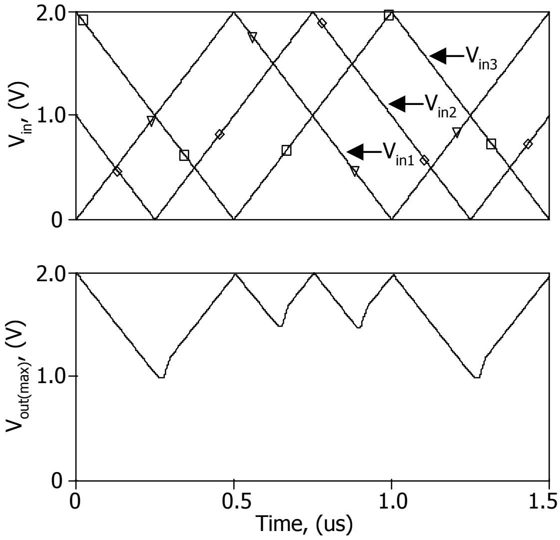

Figure 4. Transient response for three input voltages of Max circuit

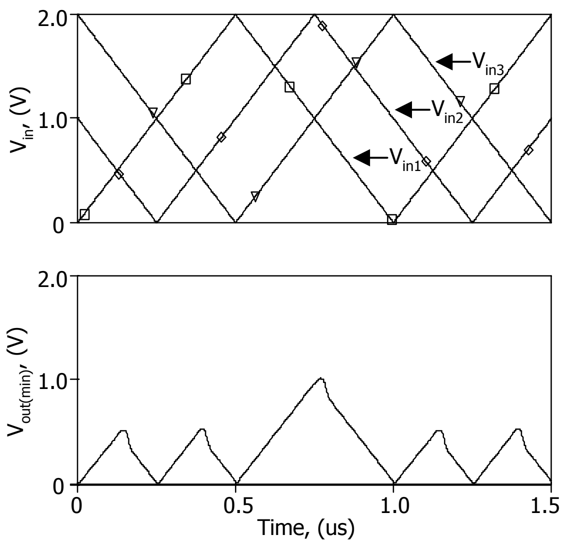

Figure 5. Transient response for three input voltages of Min circuit

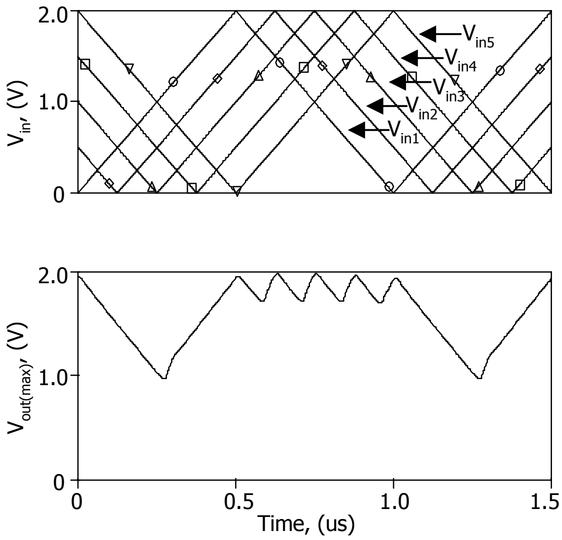

Figure 6. Transient response for five input voltages of Max circuit

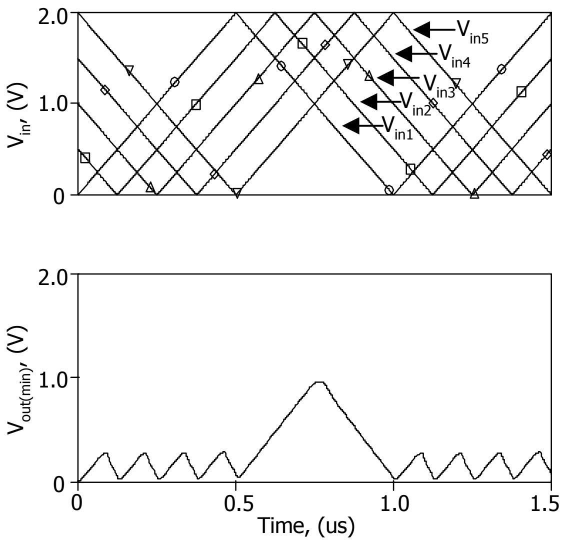

Figure 7. Transient response for five input voltages of Min circuit

4. Conclusion

In this article, a simple high-speed circuit technique for multiple-input Max and Min circuits has been presented. The realization method is based on the principle of the current conveyor configuration, which is appropriate to the real time applications. The results of the PSPICE simulation verified that the proposed Max and Min circuits have the high-speed operation.

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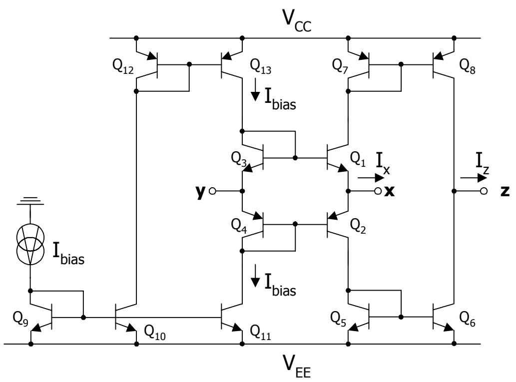

Figure 8. Schematic diagram of the CCII+ proposed in Reference [7].