

Implementation of a new stochastic neurochip and a study on transitions between limit cycles by stochastic noise

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1. Introduction

In recent years, computers and machines are being closer to our life, and the more intelligent computers are required. Neural computations seem to be appropriate for realistic jobs such as pattern recognition, optimization problems, and others. However, the system may require thousands of neurons to do such problems, and it is necessary to implement such a system on VLSI chips for practical use.

There are roughly two types of implementation way, analog and digital neuron circuits. Although the analog circuit has the advantage of the chip area, it is weak against a noise and its reliability is poor. While the digital circuit is hungry for chip area. To find a solution for such dilemma, we incorporate stochastic logic with the digital circuit. Using stochastic logic, we can satisfy both of chip area and reliability. But it was said that stochastic logic is inferior in the processing speed. In this paper, we show that this defect is not so crucial in the large system. As an important feature of the stochastic logic, it is mentioned that some kind of noise always follows on gate operations. This feature is interesting because of the similarity to a brain. To study the noise effect to the neural network, we investigate the behavior of the stochastic neural networks with cyclic connections.

2. Stochastic logic and stochastic neuron

2.1. Stochastic logic

Stochastic logic executes various complex operations in basic logic gates as using the pulse sequences that is transformed by PDM(Pulse Density Modulation) from analog (or digital) value[1]. Figure 1 shows the way to transform the analog (or digital) value X to the stochastic pulse sequence. The value X is compared with random numbers which are distributed uniformly from 0 to X_{max} ; then it fires(outputs 1) if X is smaller than X_{max} , else it doesn't fire(outputs 0). The firing probability P_f is written by the equation $P_f = X/X_{max}$, and the pulse accumulation of the pulse sequence is distributed

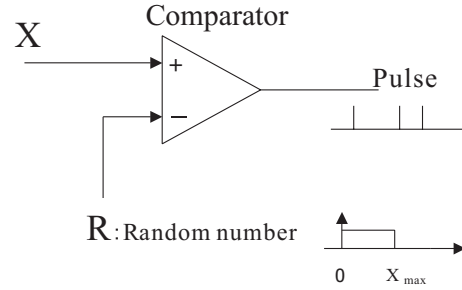


Figure 1: Coding circuit which codes a digital or an analog value in a stochastic pulse sequence

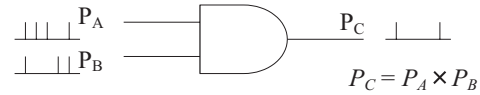


Figure 2: Stochastic multiplier using an AND-gate

by binomial distribution. Then the expectation and the variance of X after accumulation of the pulses are expressed by following;

$$E[\tilde{X}] = (X_{max}/N_a)N_a P_f = X \quad (1)$$

$$\begin{aligned} V[\tilde{X}] &= (X_{max}/N_a)^2 N_a P_f (1 - P_f) \\ &= \frac{1}{N_a} X (X_{max} - X) \end{aligned} \quad (2)$$

where X_{max}/N_a is a normalization constant. The variance $V[\tilde{X}]$ means that the pulse sequence contains noise depending on the accumulation time N_a . Figure 2 shows a stochastic multiplier using a single AND-gate. Multiplication is probably the simplest basic computing primitives for the stochastic logic, and we can make some other operation units by combination of simple logic gates.

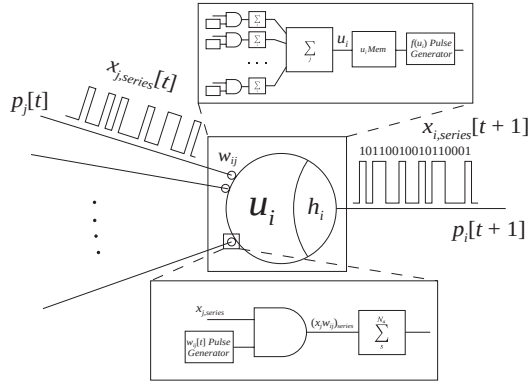


Figure 3: The block diagram of the Stochastic Neuron

2.2. Stochastic neuron

Our neuron model, stochastic neuron, was proposed by Y.Kondo *et al*[2]. Stochastic neuron is based on the fundamental discrete time neural model. Following is the mathematical expression;

$$u_i(t+1) = \sum_j w_{ij}x_j(t) + \theta_i \quad (3)$$

$$x_i(t) = f(u_i(t)) \quad (4)$$

where u_i is the i -th neuron's membrane potential, w_{ij} is the synaptic weight from j -th neuron to i -th neuron, θ_i is the threshold for firing, x_i is the output of the i -th neuron, and $f(x)$ is an activation function, respectively.

Figure 3 shows the block diagram of the stochastic neuron. In this figure, an AND-gate operates as a multiplier, a summation unit counts the number of the pulses, and a pulse generator encodes an analog(or a digital) value to a pulse sequence by the former coding method shown in Fig.1. The activation function unit generates similar stochastic pulse sequence. The firing probability is shown in figure 4.

On the same way, we can design a learning circuit for the synaptic weights. We adopt the DBM(*Deterministic Boltzmann Machine*) for learning method[3], then weight update is given by the following equation.

$$\Delta w_{ij} = \frac{\varepsilon}{T} \sum_{\alpha} \left((x_i^{\alpha} x_j^{\alpha})_{clamped} - (x_i^{\alpha} x_j^{\alpha})_{free} \right) \quad (5)$$

where ε is a learning rate, T is a gain parameter and α is the index of a visible units' pattern, respectively.

First and second stochastic neuron chip was made by Nemoto *et al*[4]. The first one includes 20 neurons and 200 synaptic weight memories. The second one includes 50 neurons and requires external memory modules. The latter chip can set up a multi-chip system, and a pair-chip system was set and measured[5]. However, the system speed was not so fast;

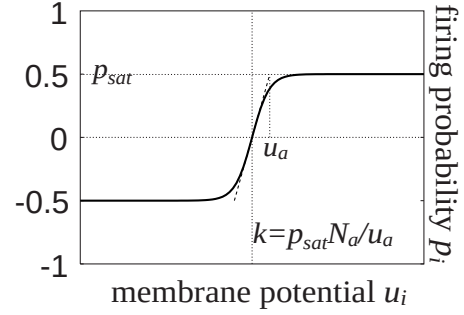


Figure 4: The characteristic of the activation function

it operated by less than 1MHz of frequency in the multi-chip system.

2.3. The performance of the stochastic neuron system

Instead of the great advantage of stochastic logic to the chip area, stochastic neuron is inferior to other implementation ways of neuron models in processing speed because it requires sufficient accumulation time N_a to decrease the effect of the noise. But we can show that the accumulation time N_a can be decreased when the network scale becomes large.

The expectaion and variance of the membrane potential of the stochastic neuron system can be expressed as follows;

$$E[u] = \bar{N}X \quad (6)$$

$$V[u] = \frac{X(X_{max} - X)}{\bar{N}N_a} \quad (7)$$

where $\bar{N}$ is the average number of neurons connect to the observable one neuron. This equation means N_a can be made smaller, for keeping the variance of the membrane potential sufficiently small, as N enlarges. The other hand, this system is able to calculate the variation of the membrane potential for all neurons simultaneously. So the operation speed rises in proportion to the network scale $\bar{N}$.

These effects make the operation speed become fast proportional to $\bar{N}^2$. Hence the disadvantage of the stochastic logic can be overcome.

3. Stochastic neurochip for multi-chip system

We design the new stochastic neuron chip which is suitable for multi-chip operation. This chip will be fabricated through VDEC, 0.35 μ m rule CMOS technology. The chip size is 4.9mm $\times$ 4.9mm, and this chip includes 64 stochastic neurons. Because the synaptic weight memories are not included, it requires external memory modules. To compose

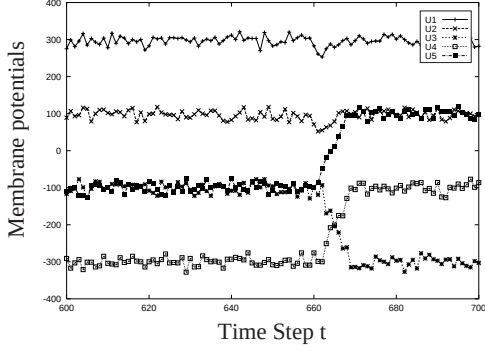


Figure 5: Changes of membrane potential on the moving co-ordinate system (gain = 1.2, $N_a = 50$, $N = 5$)

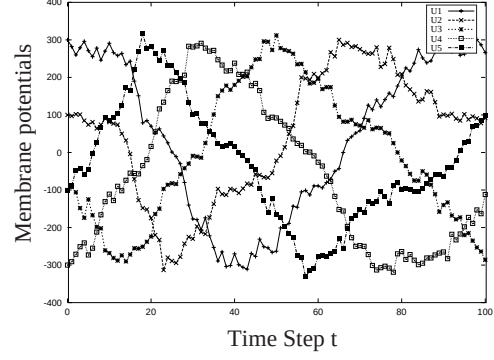


Figure 6: Changes of membrane potential on the moving co-ordinate system (gain = 0.8, $N_a = 50$, $N = 5$)

the system includes 1000 neurons, 16 pieces of this chip, and 1MB of external memory is required.

The digital circuit simulation shows that this chip operates by a maximum of 30MHz. When we construct the system of 1000 neurons and it operates by 10MHz, the neuron system demonstrates the performance of 1 [GCPS(Giga connection per second)] (assuming $N_a = 10$).

4. The behavior of the cyclic connection network on the stochastic neuron system

The stochastic behavior of our chip is interesting because such characteristics should be effective for optimization problems or improving the learning ability[6]. In this research, we investigate such effects on the limit cycles achieved with a cyclic connection network. The synaptic weights of this network is asymmetric, and neurons connect to only themselves and the nearest neighbor two neurons. It is known that the limit cycles appear in such the network on the deterministic model in both continuous and discrete time[7].

We confirm that the same limit cycles appear on our stochastic neuron system, and sufficiently small N_a causes the transition from a limit cycle to the other limit cycle. We can summarize the characteristics of such network on the stochastic neuron system as follows;

1. The transition frequency depends on the accumulation time N_a and the gain of the activation function.
2. There are stable limit cycles and unstable ones.
3. When the gain of the activation function is sufficiently small, some limit cycles, which are separate in high gain regime, merge into other limit cycle with long period.

Remarkably, the fusion phenomena, the third features in the above, appears similarly on a deterministic model. It is

similar to the behavior of the limit cycles on the continuous time analog model[8]. This phenomena probably relates to the transition frequency between the limit cycles on the stochastic model. Actually, the transitions occur frequently between the limit cycles which merge in low gain regime.

Figure 5 shows the network states on the stochastic system. Each plot shows each neuron's membrane potential in the cyclic network composed of 5 neurons. The result shows the transition of the limit cycles at the point $t = 660$. Figure 6 shows the network state when the gain is small. The periodic change appears in this condition. This transition is provided by the stochastic system, but we confirm the similar one is obtained with the deterministic system.

In Fig.7, we plot the gain - transition frequency characteristics of the 5 neuron system. The gain become smaller, the transition happens easily. Furthermore, small N_a causes increase of the transition frequency. It is easy to explain by the relation of accumulation time N_a and noise in Section 2. The transition probability in high gain limit regime P_{hl} is obtained with the variance of the membrane potential and the distance of attractors between two limitcycles.

$$P_{hl} = \frac{1}{2} \operatorname{erfc} \left(\sqrt{\frac{N_a}{6}} \right) = \frac{1}{\sqrt{\pi}} \int_{\sqrt{\frac{N_a}{6}}}^{\infty} \exp(-t^2) dt \quad (8)$$

Figure 9 shows that simulation results agree with this equation.

It is noted that simulation results show that the transitions are periodic with the gain below 1, and non-periodic with the gain above 1. The similar curve for the deterministic model in Fig.8. Under a certain gain value, the transition seems to be occurred on the deterministic model, too. It can be seen that transitions are periodic since they occur only with the gain below 1.

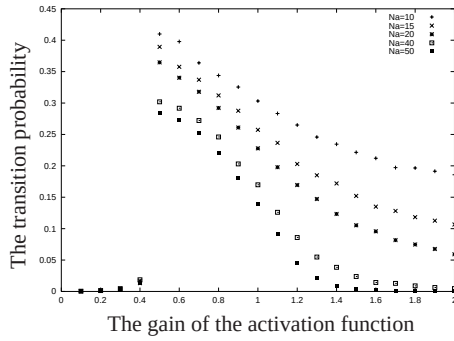


Figure 7: The probability of the transition between limit cycles on the Stochastic Model

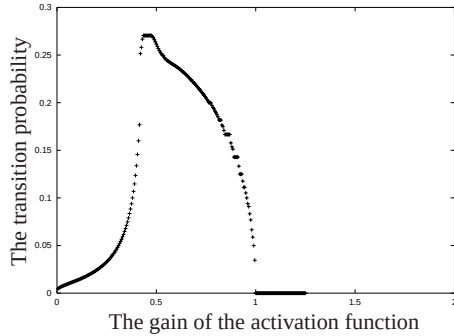


Figure 8: The probability (frequency) of the transition between limit cycles on the Deterministic Model

5. Conclusions

We show the accumulation time N_a can be decreased in inverse proportion to the network scale $\bar{N}$. So the operation speed will be improved in a large-scale system. We have designed the new stochastic neuron chip suitable for a multi-chip system based on this consideration. This chip has 64 neurons in $4.9\text{mm} \times 4.9\text{mm}$ (VDEC, $0.35\mu\text{m}$ rule), and it will operate by more than 10MHz, and this speed would be sufficient for the practical applications.

To study the effect of the stochastic noise, we investigate the limit cycles on a cyclic connection network. We confirm the limit cycles appear on the stochastic neuron system similarly to the deterministic and discrete-time model neuron system. Especially on the stochastic model, we confirm the transition between limit cycles, and its frequency depends on N_a and the gain of the activation function. It is interesting that some limit cycles merge to a unified long period limit cycle when the activation function has low gain either on the stochastic or on the deterministic model. And the transition frequency on the stochastic model probably relates to this phenomenon.

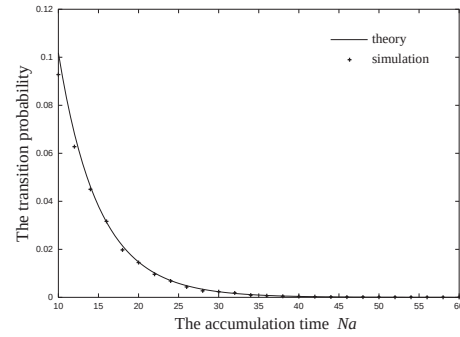


Figure 9: The transition probability in high gain limit regime on the 5 neuron stochastic system

6. Acknowledgments

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