An IC Implementation of Asynchronous Pulse Neuron Model

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Abstract – An asynchronous pulse neural network, which processes fine timings of many action potential pulses, has been proposed. This paper describes an IC implementation of the model. The circuit is designed and laid out using MOSIS HP/Agilent 0.5 μm CMOS semicondactor process. HSPICE simulation results of the prototype chip is shown.

1 Introduction

Information processing in the brain utilizes action potential pulses among neurons. Especially, information cording using the spacio-temporal structure of action potential pulses has received much attention. A neural network model based on spacio-temporal cording [1]-[3], the pulse propagation network and asynchronous chaotic neural network have been investigated [4].

The neuron in these models works asynchronously as a coincidence detector of incoming pulses. Moreover, the dynamical cell assembly formations have been demonstrated. Advantages for a hardware implementation of such neuron models include fast processing speed and suitability for trial-and-error testings.

However, an IC implementation of such neural network models has difficulty, because input and output pulses are impulses. To overcome this problem, the asynchronous pulse neural network model has been proposed, which employs a pulse with finite width in order to be fit to an analog circuit implementation [4, 5].

In this paper, the asynchronous pulse neural network model is implemented as an analog integrated circuit. The state variables and timing of the integrated neuron are all continuous, so that the circuit faithfully realizes the model. Moreover, it is possible to alter the parameters of the model such as the resting potential, threshold voltage and synaptic delay using the external bias voltages. Furthermore, the extrapolated internal state value [4] and the absolute refractory period are also implemented in the integrated circuit. All the state variables and action potential pulses can be observed.

The integrated neuron circuit can function both as a coincidence detector and as an integrator by adjusting its internal time-constant with the external bias voltage.

The chip employs wide-swing buffer and current mirror circuits to realize a rail-to-rail operation. The size of the MOSFET resistor in the SOMA circuit (See Fig. 3) is carefully chosen in order to obtain a wide internal time-constant range. As a result, various complex behaviors including chaotic responses can be realized [4].

In section 2, a short explanation of the asynchronous pulse neural network model is given. Section 3 explains the circuit implementation of the asynchronous pulse neuron model. Finally in section 4, simulation results with HSPICE are shown.

2 Asynchronous Pulse Neuron Model [4]

The time responses of the model is shown in Fig. 1.

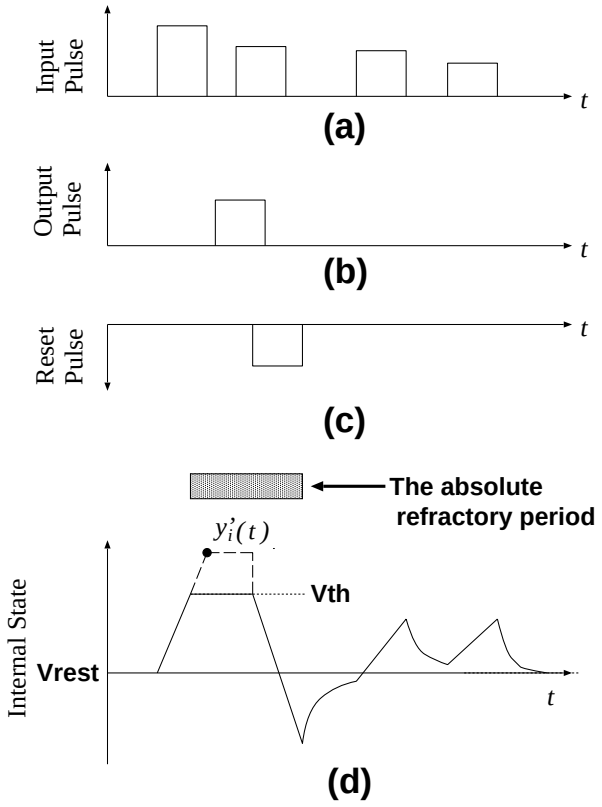


Figure 1: Time responses of the model neuron. (a) Input pulses, (b) output pulse, (c) reset pulse and (d) intarnal state.

As a pulse comes into the neuron, the internal state changes linearly at the rate which depends on the strength of the synaptic connection. When the internal state reaches to the firing threshold, Vth, the neuron fires and an output pulse is generated. Then, a reset pulse is generated. During the existence of the reset pulse, the internal state decreases linearly. Once the neuron fires, the absolute refractory period begins and continues until the reset pulse disappears. Any input pulse during this period is ignored. Without any input pulse, the internal state decays exponentially to the resting voltage, Vrest. To introduce the strength and time dependencies of the output and reset pulses on the characteristics of the inputs, this model uses an extrapolated value of the internal state, y_i' [4].

3 Circuit Implementation

The synapse circuit and soma circuit are shown in Figs. 2 and 3, respectively.

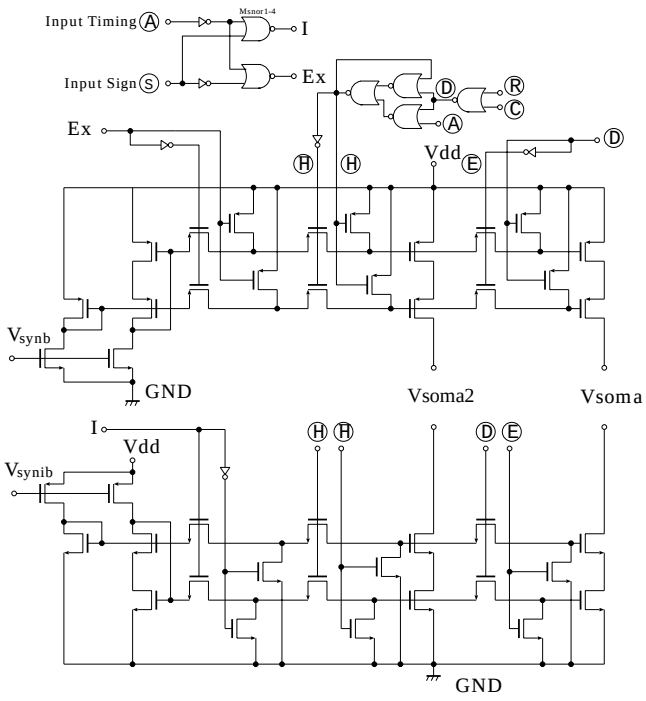


Figure 2: The synapse circuit.

The synapse circuit consists of two parts, that is, inhibitory and excitatory connections. One of these connections is selected through a digital circuitry shown as I and Ex in the figure. When the corresponding connection is chosen, the capacitors in the soma circuit, Csoma and Csoma2, are either charged or discharged linearly. The voltages at Csoma and Csoma2 represent the internal state of the neuron and the extrapolated value [4], respectively. The charge or discharge current can be changed with external bias voltage by which the synaptic weight is altered.

The soma circuit in Fig. 3 contains a wide-swing buffer circuit. The buffer circuit makes Vsoma2 and Vsoma equal when the reset pulse ends.

A MOSFET resistor consists of an N-MOS and P-MOSFETs is placed in parallel to the soma capacitor, Csoma. The internal time-constant of the neuron can be adjusted by changing the gate voltages of this CMOSFET resistor, Vb3 and Vb4. Vrest defines the resting potential.

The relative refractoriness circuit is shown in Fig. 4. When the reset pulse rises up, the MOSFET-switches in the current-mirror are closed by signal R, then the current flows through the the current-mirror circuit discharging Csoma. Relative refractoriness strength depends on the output voltage of the sigmoidal function circuit [4]. The dependency can be controlled with the 3-bit external signal, Va, Vb and Vc. The current-mirror circuit has a wide-swing structure to realize the rail-to-rail operation.

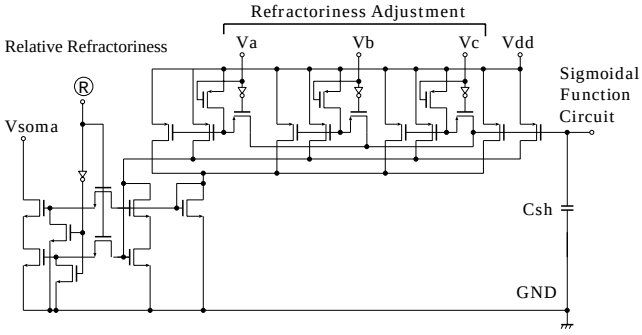


Figure 4: The relative refractoriness circuit.

The sigmoidal function circuit and comparator are shown in Fig. 5. This circuit consists of a differential amplifier and two CMOS inverters. When Vsoma2 crosses over the threshold voltage, Vth, the output of the comparator rises, and the output pulse and reset pulse are generated at the pulse generators shown below. The delay of the output pulse depends on the output voltage of the differential amplifier. The shape of the sigmoidal function can be changed with the external voltage, V_{bn_out}.

The output pulse generator circuit is shown in Fig. 6, which consists of a current-mirror, a Schmitt trigger and a CMOS inverter. When the output of the comparator rises, the MOSFET switches in the current-mirror close. The width of the output pulse can be changed with the external voltage, V_{bw_out}. The reset pulse generator is very similar to the output pulse generator, so it is not shown in this paper.

The prototype chip is designed using MOSIS HP/Agilent 0.5 μm CMOS process. The chip contains a neuron circuit and testing circuits. The testing circuits are designed so that the characteristics of each component of the neuron circuit can be evaluated separately. The layout of the chip is shown Fig. 7

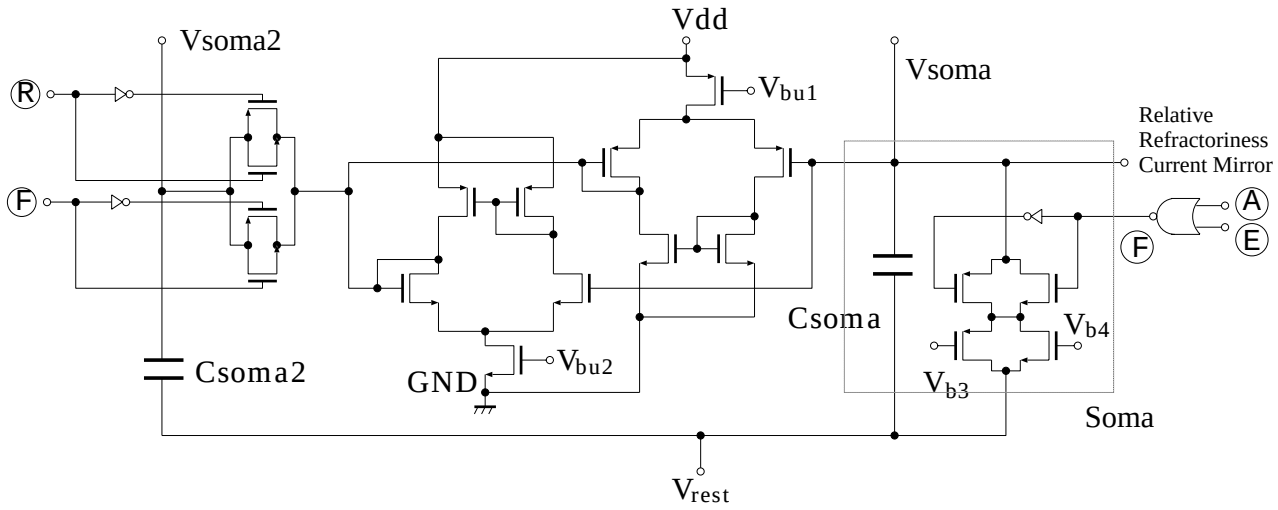


Figure 3: The soma circuit and buffer circuit.

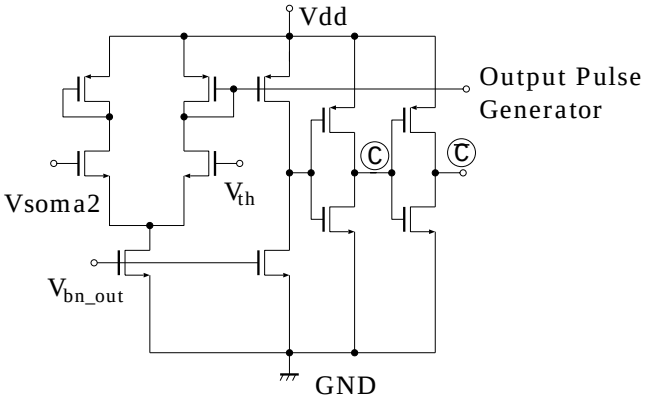


Figure 5: The sigmoidal function circuit with comparator.

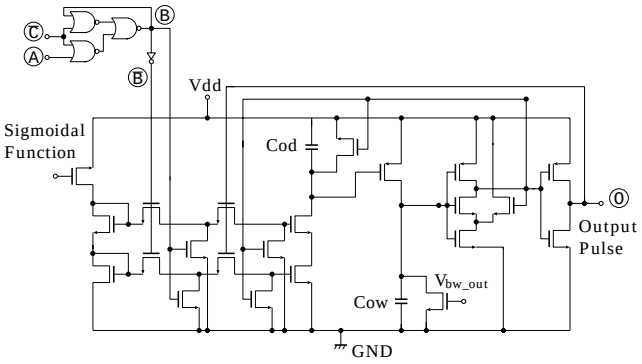


Figure 6: The output pulse generator circuit.

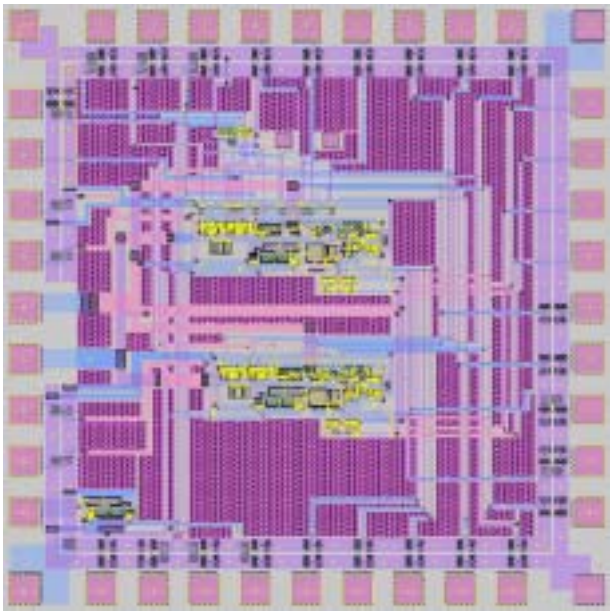
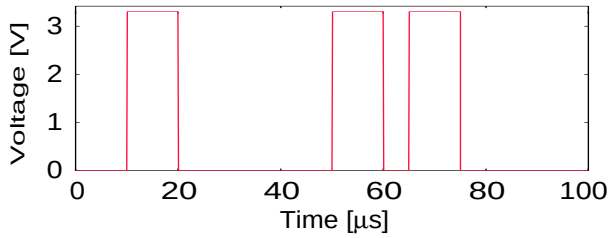


Figure 7: Layout of the prototype chip.

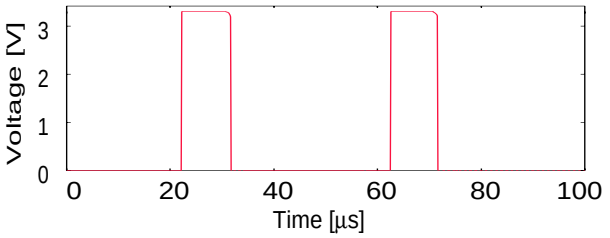
4 Simulation Results

The designed circuit is simulated using HSPICE circuit simulation program. Figure 8 shows time responses of the neuron circuit. The input pulses, the internal state, the extrapolated internal state, the reset pulses and the output pulses are shown in the figure. It also shows existence of the absolute refractory period.

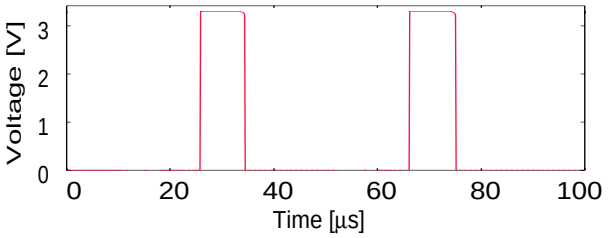
A bifurcation diagram of the amplitude of the internal state is shown in Fig. 9. Periodic pulse train with period T is applied. T is a bifurcation parameter. These results confirm that the designed neuron circuit replicates the original asynchronous pulse neuron model.



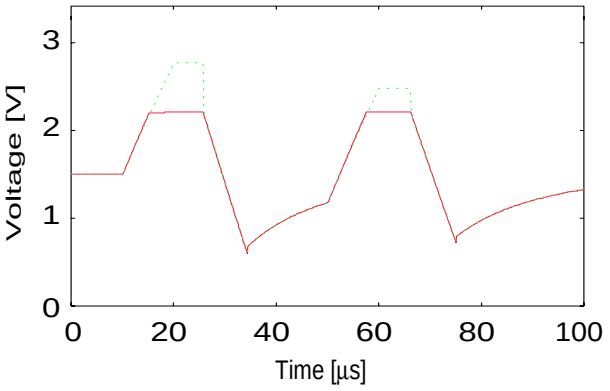
(a)



(b)



(c)



(d)

Figure 8: HSPICE simulation results of the asynchronous pulse neuron circuit. (a) Input pulse, (b) output pulse, (c) reset pulse and (d) internal state, Vsoma.

5 Conclusions

In this paper, an analog integrated circuit based on the asynchronous pulse neuron model has been proposed. Simulation results of the circuit with HSPICE show that the proposed circuit exhibits qualitatively similar characteristics to the original model.

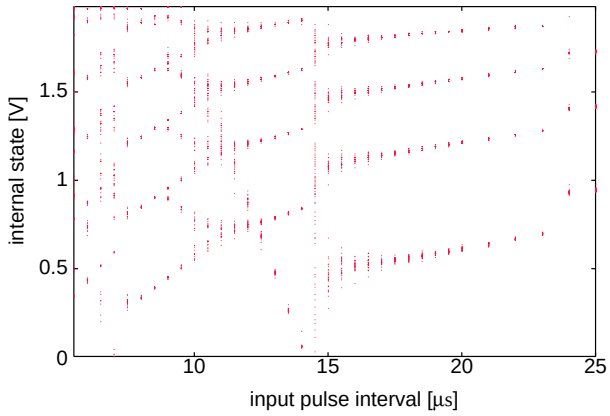


Figure 9: A bifurcation diagram of the internal state.

As a future problem, we will design a network using the proposed circuit.

References

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