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An Analog CMOS Current-mode Sorting Circuit

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Abstract: A CMOS-based maximum and minimum operations cell to compare two input currents is described. Using this cell as a basic unit, a four-input sorter is designed. The outputs are obtained by ordering the inputs in the decreasing order. This sorting circuit has a simple and flexible structure. The procedure can be extended to design an n-input sorter. The performances of the proposed circuit were studied by the use of the PSPICE analog simulation program. The simulation results verified the circuit performances are agreed with the expected values.

1. Introduction

The principle of fuzzy circuit is based on "Sum-Sorting" rule [1]. In fuzzy circuit, membership function generators employ current-mode circuit to generate memberships corresponding to each standard pattern according to input features. Switched-current accumulators are adopted to realize the Sum function to get synthetic memberships. Sorting circuit sorts all of synthetic memberships based on their magnitudes and find out standard patterns closer to unknown pattern [2], and finally recognition results are outputted. At present, many sorting integrated circuit have been proposed, however, almost of them are digital sorting circuit [3] – [6]. Although digital sorting circuits can also used for analog signals, A/D and D/A converters are required, so that the structure of circuits will be even more complicated. Evidently, an analog signal sorter would be much faster. In addition, errors may occur in the conversion between digital signals and analog signals. To this end, an analog current-mode sorting circuit is proposed in this paper. The realization method is suitable for fabrication using CMOS technology. The proposed sorting circuit is able to output the input currents in a sorting order on the basis of the magnitudes of the input currents. The inputs to the sorter are currents i_{in1}, i_{in2}, …., i_{ink}. The outputs are i_{o1}, i_{o2}, …., i_{ok}, obtained by ordering i_{in1}, i_{in2},…., i_{ink} in decreasing order of magnitudes. To facilitate explanation, we assume that k = 4. We also assume that the input currents are in the range zero to 20μA.

2. Max/Min Cell

A maximum (Max) and minimum (Min) cell or Max/Min cell is the analog CMOS two-input maximum and minimum operations scheme [10]. The circuit diagram of Max/Min cell is shown in figure 1. The transistors are all matched and operated in their saturation regions. The transistors M_1-M_4 (CM_1), M_5-M_6 (CM_2) and M_7-M_8 (CM_3) function as unity gain positive current mirrors. The transistors M_9-M_{10} (CM_4), M_{11}-M_{12} (CM_5), M_{13}-M_{14} (CM_6) and M_{15}-M_{16} (CM_7) function as the unity gain negative current mirrors. The transistors M_{17} and M_{18} function as a current follower and, at the same time, provide a fixed bias voltage to node IP_1 and IP_2, respectively, which in this case is approximately at earth potential. The transistors M_{19}-M_{20} form an electronic switch. The transistor M_{21} and the bias current source I_1 generate a constant voltage to provide a pre-bias M_{19} and M_{20}, and bring them to the edge of conduction. The operation of the proposed circuit can be explained as follow. The current i_{D1} and i_{D5} can be stated as

$$i_{D1} = i_{in1} + I_2 \tag{1}$$

$$i_{D5} = i_{in2} + I_2 \tag{2}$$

The positive current mirrors CM_1 and CM_2 and the negative current mirror CM_4 force $i_{D1} = i_{D2} = i_{D3} = i_{D4}$, $i_{D5} = i_{D6}$ and $i_{D6} = i_{D10}$, respectively. Then, from eqns (1) and (2) can be rewritten as

$$i_{D1} = i_{D2} = i_{D3} = i_{D4} = i_{in1} + I_2 \tag{3}$$

$$i_{D5} = i_{D6} = i_{D10} = i_{in2} + I_2 \tag{4}$$

At node A, the current i_{diff} is equal to

$$i_{diff} = i_{D10} - i_{D2} = i_{in2} - i_{in1} \tag{5}$$

During $i_{in2} > i_{in1}$ or a positive difference input current $i_{diff} > 0$, the current $i_{diff} > 0$ flows through the transistor M_{19} that cause the source-gate voltage of the transistor

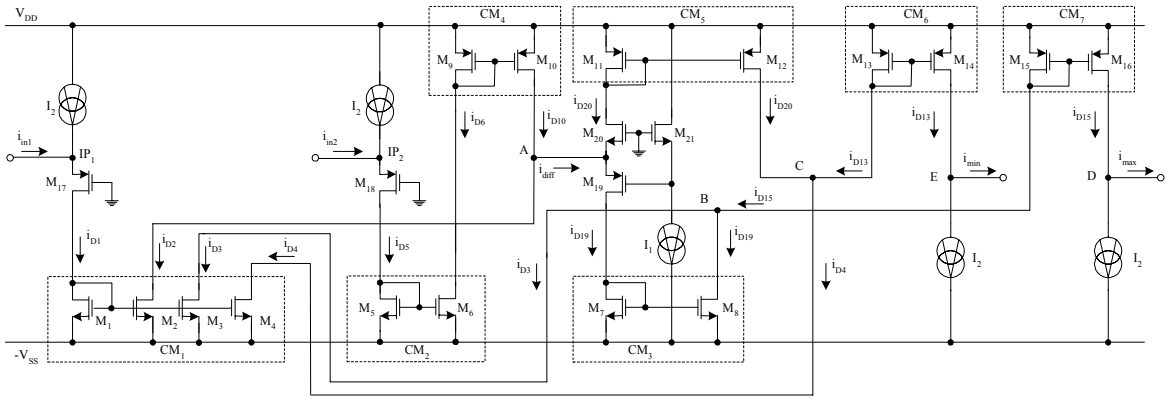


Figure 1. Max/Min Cell

M_{19} to increase and the gate-source voltage of the transistor M_{20} to decrease effecting M_{20} to cutoff. Similarly, the flow of a negative difference input current $i_{diff} < 0$ through the transistor M_{20} causes the transistor M_{19} to cutoff. Therefore the current i_{D19} and i_{D20} can be given by

$$i_{D19} = \begin{cases} i_{diff} & ; i_{in2} > i_{in1} \\ 0 & ; i_{in1} \geq i_{in2} \end{cases} \quad (6)$$

$$i_{D20} = \begin{cases} 0 & ; i_{in2} \geq i_{in1} \\ -i_{diff} & ; i_{in1} > i_{in2} \end{cases} \quad (7)$$

The positive current mirror CM_3 and the negative current mirror CM_5 reflect i_{D19} and i_{D20} to node B and node C, respectively. Then the current i_{D15} and i_{D13} are given by

$$i_{D15} = i_{D3} + i_{D19} = i_{in1} + I_2 + i_{D19} \quad (8)$$

$$i_{D13} = i_{D4} - i_{D20} = i_{in1} + I_2 - i_{D20} \quad (9)$$

The current i_{D15} and i_{D13} mirror to node D and E by and the negative current mirror CM_7 and CM_6, respectively. Then the maximum current i_{max} and minimum current i_{min} can be stated as

$$i_{max} = i_{D15} - I_2 = i_{in1} + i_{D19} \quad (10)$$

$$i_{min} = i_{D13} - I_2 = i_{in1} - i_{D20} \quad (11)$$

Substituting eqns. (6) and (7) into (10) and (11) respectively, the output current i_{max} and i_{min} can be written as

$$i_{max} = \begin{cases} i_{in2} & ; i_{in2} > i_{in1} \\ i_{in1} & ; i_{in1} \geq i_{in2} \end{cases} \quad (12)$$

$$i_{min} = \begin{cases} i_{in1} & ; i_{in2} \geq i_{in1} \\ i_{in2} & ; i_{in1} > i_{in2} \end{cases} \quad (13)$$

It is clearly seen that the Max/Min cell has the maximum and the minimum operations of two-input currents.

3. Four-Input Sorter

For convenience, a current-mode sorting circuit based on magnitude is discussed by taking four input currents for example. The circuit diagram of the four-input sorter is shown in figure 2. The inputs to the circuit are designed i_{in1}, i_{in2}, i_{in3} and i_{in4}. The outputs of the circuit are designed i_{o1}, i_{o2}, i_{o3} and i_{o4}. The outputs are obtained by ordering the inputs in the increasing order. For the purposes of illustration, let i_{in1} = 10μA, i_{in2} = 20μA, i_{in3} = 15μA and i_{in4} = 5μA. Consequently, i_{o1} = 20μA, i_{o2} = 15μA, i_{o3} = 10μA and i_{o4} = 5μA (see figure 3.)

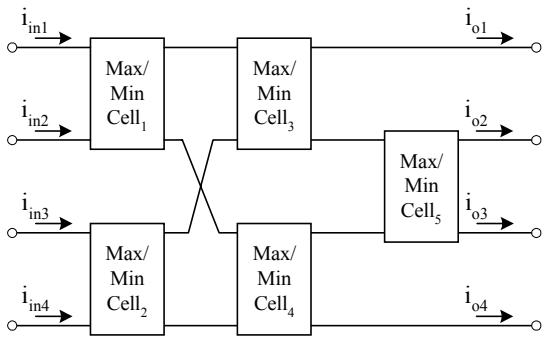


Figure 2. A Four-input Sorter

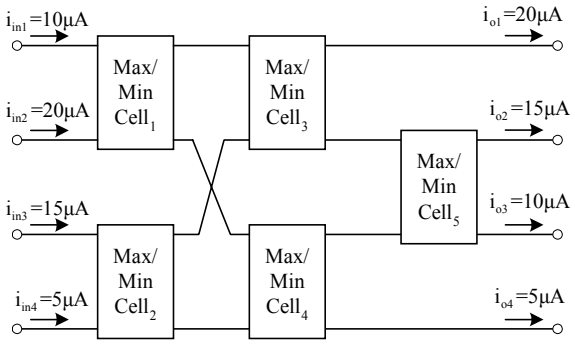


Figure 3. Example Problem

The number of comparison elements increases rapidly with k, the number of input currents. A formula for the minimum number of comparison elements for a given k is not known. However, [8] contains a list of best upper bound values known for values of k for 3 to 16. For example, the minimum number of comparison elements when k = 6 is 12. The sorting network for k = 6 or a six-input sorter is shown in figure 4.

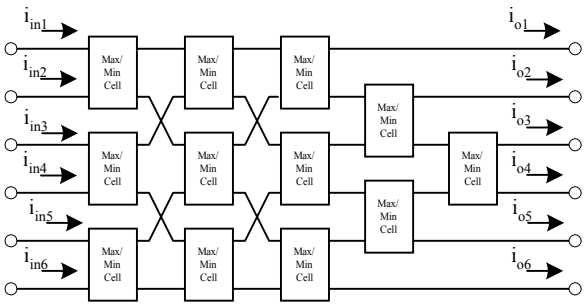
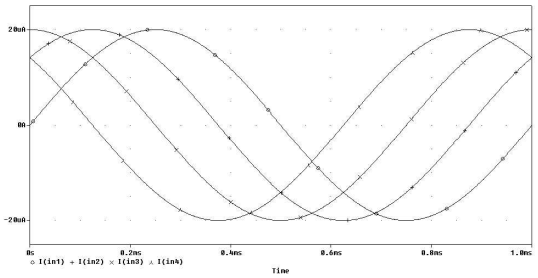


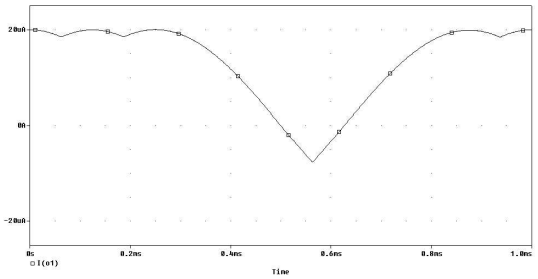
Figure 4. A six-input sorter

4. Simulation Results

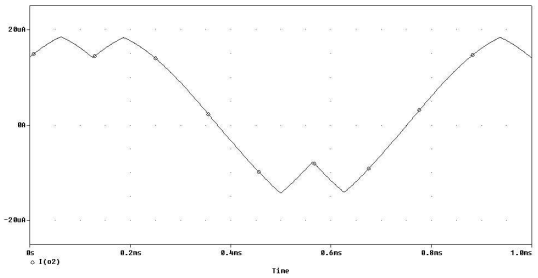
The performances of the proposed four-input sorter were studied by the use of the PSPICE analog simulation program. The BSIM MOS model of the 0.7μm CMOS process was used for the circuit simulation. The Max/Min as shown in the figure 1, the dimension W/L of the devices used are 10μm/1μm, the bias currents I_1 and I_2 are set to 50μA and $V_{DD} = -V_{SS} = 2.4V$. Figure 5 shows the simulated transient response for the 1kHz sinusoidal, where the input currents i_{in1}, i_{in2}, i_{in3} and i_{in4} are 20μA peak amplitude with 0°, 45°, 90°, 135° phase shift, respectively. Figure 6 shows the simulated transient response for the triangular input signal currents, where i_{in1}, i_{in2}, i_{in3} and i_{in4} are 20μA peak amplitude and 1.0ms time period. It is evident that the proposed circuit has correct function and good performances.



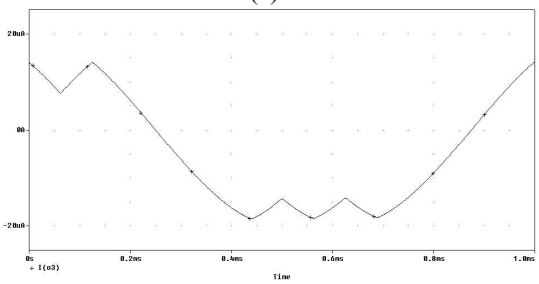
(a)



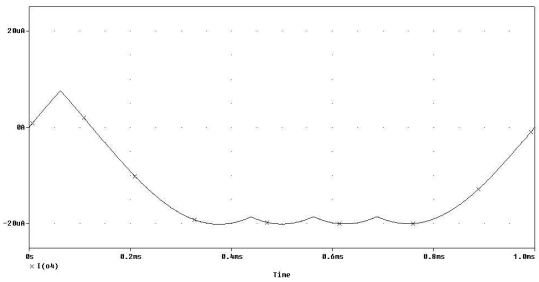
(b)



(c)

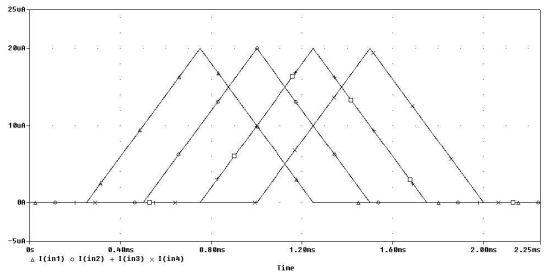


(d)

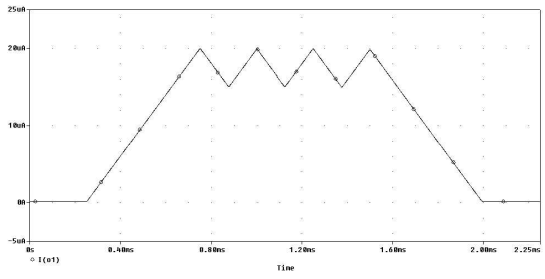


(e)

Fig. 5. Simulated transient response of the 4-input sorter
(a) 1kHz Sinusoidal input signal currents
(b) the output current i_{o1}
(c) the output current i_{o2}
(d) the output current i_{o3}
(e) the output current i_{o4}



(a)



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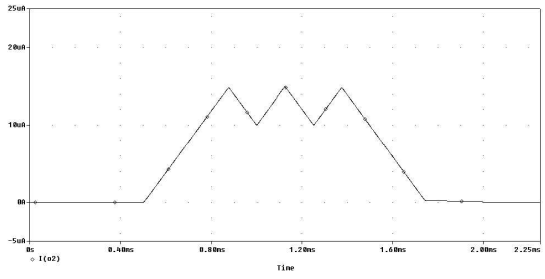

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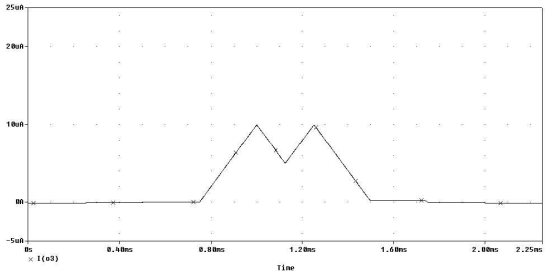

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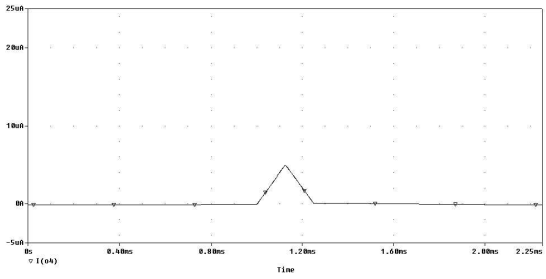

(e)

Fig. 6. Simulated transient response of the 4-input sorter
(a) Triangular input signal currents
(b) the output current i_{o1}
(c) the output current i_{o2}
(d) the output current i_{o3}
(e) the output current i_{o4}

5. Conclusion

Based on the above design, the proposed current mode sorting circuit was tested for all input conditions including those for which two or more of the input are equal. The proposed sorter has correct function and good performances. It has a simple, flexible structure and is able to directly fabricated in a standard CMOS process. A sorter with more input currents can be design on similar lines.

Acknowledgments

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