HDL SYNTHESIS AND SIMULATION OF SIGNED SIXTEEN BIT FIXED POINT HIGH SPEED ARCHITECTURE FOR TWO-DIMENSIONAL RECURSIVE FILTERS

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Abstract

This paper describes two dimensional State space filter algorithms and proposes Folded architecture for high speed image processing applications by exploiting the inherent spatial concurrency of systolic arrays. Global Speed up architecture (GSR), which is discussed in this paper, has an array of forty nine processing elements with a through put rate of one pixel per clock period.. In the proposed folded architecture, we have reduced the number of processing elements to seven, maintaining the same through put rate of one pixel per clock period. Each processing element or basic cell has signed fixed point adder and multiplier and accumulator. For the first seven clock cycles, the same basic cell is used for processing a column of seven pixels and is fed as output to second column's basic cell at eight clock pulse. Output will be coming out of second column at start of fifteenth clock pulse. In this way, at the end, forty ninth clock pulse output will be available in all the seven column processors achieving a through put rate of one pixel per clock cycle. The core has been designed using VERILOG as the HDL language and synthesized with FPGA logic unit which targets FPGA SPARTAN S05VQ100 at frequency of 50 MHz

1.0 Introduction

In linear systems, a given transfer function can be realized by a variety of structures. A 2D state-space structure can realize IIR digital filters with minimum round off noise[1] – [6]. Different realizations of a given filter will have the same linear response, but may have different hardware complexity and different finite word length.In the past few years, high speed image processing using digital filters has become a rapidly growing field, as the need for fast processing is evident. Many applications involve acquisition, transmission, processing and display in the real time. In these areas, each pixel has to be processed in a very short time, inversely propotional to the data rate that is very high. Therefore several architectures for digital image processing are developed.

2.0 Local State-Space Realization of 2-D Recursive filter

A single input single output 2-D digital filter can be represented by the local state space model

$$\begin{pmatrix} x^h(i+1,j) \\ x^v(i,j+1) \end{pmatrix} = \begin{pmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{pmatrix} \begin{pmatrix} x^h(i,j) \\ x^v(i,j) \end{pmatrix} + \begin{pmatrix} b_1 \\ b_2 \end{pmatrix} U(i,j) \qquad \ldots (1)$$

$$y(i,j) = (c1,c2) \begin{pmatrix} x^h(i,j) \\ x^v(i,j) \end{pmatrix} + du(i,j) \qquad \ldots(2)$$

Where I=0,1,….., N-1, j=0,1,….. m-1

U (i,j) and y(i,j) are the input and the output respectively. $x^h(i,j)$ is the horizontal state-space vector component of dimension (nx1), and $x^v(i,j)$ is the vertical component of dimension (mx1). A is an [(n+m) x (n+m)] matrix. n and m are dependent upon the number of delay operators in the horizontal direction and in the vertical direction respectively of a signal flow graph. For a second order filter, n=2, m=4, or n=4,m=2, based on the different forms of the signal flow graph and k=7.

To obtain a filter with minimum round-off noise, low coefficient sensitivity and free of overflow oscillations, the coordinate transformations have to be used to produce well designed state space structures, which minimize the finite word length effects. In general, after transformations, the resultant matrices will not be sparse, Accordingly, a realization with minimum round-off noise will require more multipliers, at most k^2(k=n+m+1) multipliers. Therefore the improvement in the finite word length effects is obtained at the expense of an increase in hardware complexity.

2.1 Drawbacks Local State-Space Realization of 2-D Recursive filter

According to the state equations (1) and (2), for each given x(i,j) and u(i,j), we have to find the horizontal state vector, x^h (i+1,j) and the vertical state vector x^v (i,j+1) as well as computing the output y(i,j). It is shown in that due to the recursive property, the pixel at (I+1,j) or (I,j+1) can not be processed until x^h (i+1,j) or x^v (i,j+1) are available. The problem is that with the regular scanning method, the input data have to be interleaved by zeros. Therefore, during the filtering process, most of the processing elements in the array will be idle. The efficiency is 1/k. The throughput rate and improve the efficiency, the input and output have to be rescanned along the diagonal direction.

3.0 Global Speed up Architecture.

The global speed-up structure consists of forty nine processing elements. These elements are grouped as seven column processors. They are called as column processors because they are suitable for processing images along the vertical directions. Each processor contains each processing cells, and each cell consists of a multiplier, an adder, shift registers, 1 latch and 2-D flip-flops. In this design, the input u(ij) and the components of the state vector remain at the cells of the array for seven clock periods. The coefficients of each row in the matrix circulate around each cell of the array. The partial results move systolically from cell to cell in the up to down direction. After a delay of seven clocks, the final values of y(i,j), $X_1^h(i,j)$, $X_2^h(i,j)$, $X_1^v(i,j)$, are obtained from the bottom at the rate of one output per clock and repeated for other column cells

4.0 VLSI IMPLEMENTATION OF FOLDED ARCHITECTURE

In the proposed Folded architecture we have reduced the number of processing elements to seven maintaining the same through put rate of one pixel per clock period. Each processing element or basic cell has signed twenty-four bit fixed-point adder and multiplier. Signed sixteen bit filter coeeficients are stored in an array of forty nine ROM cells. During each clock pulse, the pixel value and the coefficient value varies, depending on the position of the pixel on the global speed structure. The pixels in the first row of each column get their pixel values from the input stored in the ROM.

Each processing element or basic cell has signed fixed-point adder and multiplier and accumulator. For the first seven clock cycles, the same basic cell is used for processing a column of seven pixels and is fed as output to second column's basic cell at eight-clock pulse. Output will be coming out of second column at start of fifteenth clock pulse. In this way, at the end, forty ninth clock pulse output will be available in all the seven column processors achieving a through put rate of one pixel per clock cycle.

5.0 Results and Conclusion

According to the architecture shown in fig:2 ,the proposed two dimensional recursive filter based on Folded architecture was designed by Verilog –HDL , where a maximum of sixteen bit data can be stored as filter co efficient. The proposed circuit was synthesized with FPGA logic unit which targets FPGA SPARTAN S05VQ100 at frequency of 50 MHz.. Functional simulation result is shown in figure 3.X17, X27,X37,X47,X57,X67,X77 represent the inputs to column processors and Y17,Y27,Y37,Y47,Y57,Y67,Y77 represents the output coming out of the column processors. We find that after forty nine clock cycles output starts coming out of all the column processors and at a through put rate of one pixel per clock pulse.

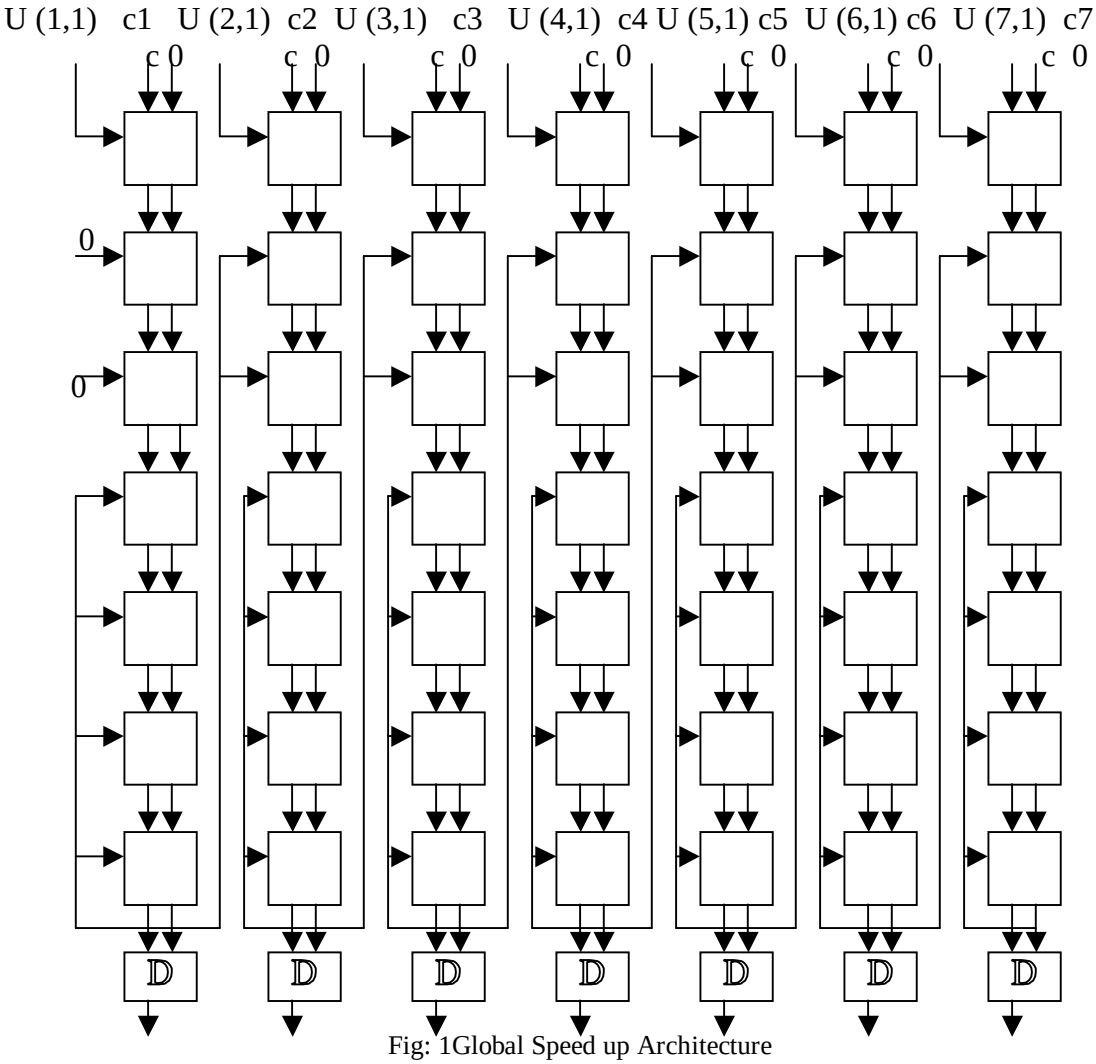

Fig: 1Global Speed up Architecture

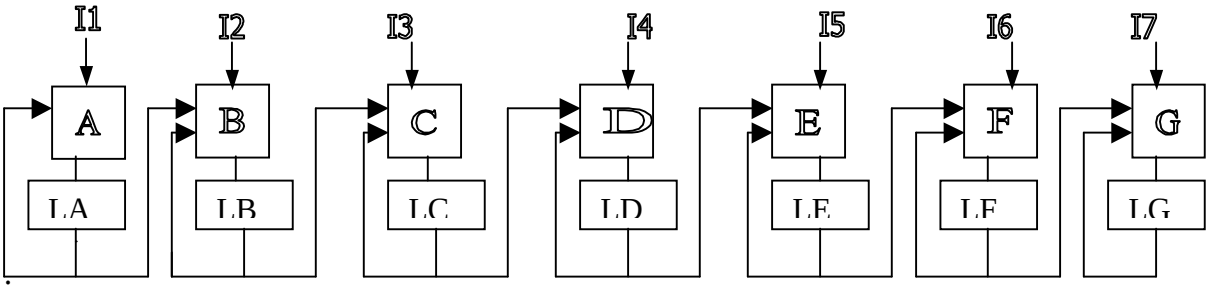

Fig 2: Folded Architecture

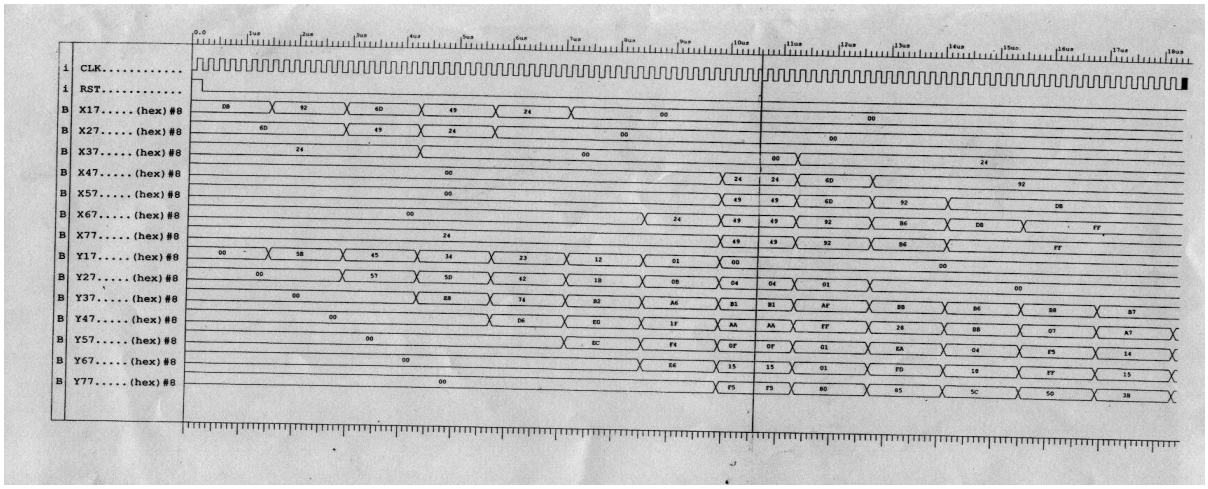

Fig 3: Functional Verification of Folded Architecture by HDL Simulation

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