AWAD2023 Program

Monda	av, July	TO		
			g Remarks	
SESSI	ON 1 : A	dvance	d semiconductor technologi	ies & Nano, 2D materials, wearable devices
	co-chaiı	·	T. Suwa (Tohoku Univ.), Se	eongjae Cho (Ewha Womans Univ.)
10:15	10:35	I-1	Taiichi Otsuji	Tohoku Univ.
				plasmons and their terahertz device applications
10:35	10:55	I-2	Young Joon Hong	Sejong University
				fabricating high-density full-color micro-LEDs
10:55	11:10	0-1	Seungwon Go	Sogang University
10.55	11.10	0-1	Investigation on Ferroelect	ricicty in Zr-doped HfO2 (HZO) based Lamianated Structure with TEMA-Hf and Cp-Zr
			Hudzaifah Al Hijri	Shizuoka University
11:10	11:25	0-2	-	wer of Flexible Thermoelectric Power Generators Based on Conductive Fabrics
11.05	11.40	0.0	Naoki Matsuda	AIST
11:25	11:40	O-3	Surfactant-free gold nanop	particle dispersed aqueous solution for surface-enhanced Raman scattering spectroscopy
11:40	13:00	Lunch	break	
				chnologies & Neuromorphic devices and computing technologies
	co-chaiı		T. Futase (Western Digital)	
13:00	13:20	I-3	Akira Fujiwara	NTT
				licon single-electron pumps Kyung Hee University
13:20	13:35	O-4	Kim Dong Hee 3-Terminal Synapse Transi	istor Array Architecture Based on HfO2 Electrolyte Gate Insulator for Implementing Synaptic Weighted-Sum Operation
			Seiya Kasai	Hokkaido Univ.
13:35	13:50	0-5	•	tion From Myoelectric Signals Based On Reservoir Computing Framework
13:50	14:05	Break		
SESSI	ON 3 : P	ower el	ectronic devices & Compou	nd semiconductor and wide bandgap devices
	co-chaiı	·	T. Terashima (Mitsubishi E	lectric), Sang Won Yoon (Hanyang Univ.)
14:05	14:25	1-4	Hyun-Seop Kim	Kunsan National Univ.
				n Substrate Bias in AlGaNGaN-on-Si Structures
14:25	14:40	O-6	Gokhan Atmaca	Hongik University
			· .	MOSFETs with BeO Gate Dielectric
14:40	14:55	0-7	Yusaku Magari High-mobility In203:H thin	Hokkaido University films and thin-film transistors deposited under varied base pressure by pulsed laser deposition
			Myeongsu Chae	Hongik University
14:55	15:10	O-8		on of p-GaN gate HEMTs under forward gate voltage stress
15:10	15:25	Break		
			iversary	
	co-chaiı	r	S. Ohmi (Tokyo Tech), W. `	Y. Choi (Seoul National Univ.)
15:25	15:55	S-1	Hideo Hosono	Tokyo Tech
10.20	10.00		Birth and Progress of IGZO)-TFTs
15:55	16:25	S-2	Tsunenobu Kimoto	Kyoto University
			•	SiC Power Devices for Higher Energy Efficiency
	16:55	S-3	Ho-Young Cha Gallium nitride power devic	Hongik University
16:25			Gamum mitrue power devic	
16:25			Tamotsu Hashizuma	Hokkaido University & Nagova University
16:25 16:55	17:25	S-4	Tamotsu Hashizume MOS technologies for GaN	Hokkaido University & Nagoya University power transistors
16:55	17:25 17:45		Tamotsu Hashizume MOS technologies for GaN	
16:55 17:25	17:45	Break		
16:55 17:25 17:45	17:45 <mark>19:30</mark>	Break Networ	MOS technologies for GaN	
16:55 17:25 17:45 Tuesd	17:45 <mark>19:30</mark> ay, July	Break Networ 11	MOS technologies for GaN king Session (Lounge)	
16:55 17:25 17:45 Tuesd SESSIG	17:45 19:30 ay, July DN 5 : M	Break Networ 11 10S logi	MOS technologies for GaN king Session (Lounge) c and memory devices 1	power transistors
16:55 17:25 17:45 Tuesd SESSI(17:45 19:30 ay, July DN 5 : M co-chain	Break Networ 11 10S logi	MOS technologies for GaN king Session (Lounge) c and memory devices 1	
16:55 17:25 17:45 Tuesd SESSIC	17:45 19:30 ay, July DN 5 : M	Break Networ 11 10S logi	MOS technologies for GaN [•] king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.),	power transistors Garam Kim (Myongji Univ.) AIST
16:55 17:25 17:45 Tuesd SESSIC 9:30	17:45 19:30 ay, July DN 5 : M co-chain 9:50	Break Networ 11 IOS logi	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim	power transistors Garam Kim (Myongji Univ.) AIST 2 as Emerging Memory Sogang University
16:55 17:25 17:45 Tuesd SESSIC	17:45 19:30 ay, July DN 5 : M co-chain	Break Networ 11 10S logi	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne	power transistors Garam Kim (Myongji Univ.) AIST 2 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology
16:55 17:25 17:45 Tuesd SESSIC 9:30	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10	Break Networ 11 IOS logi	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong	power transistors Garam Kim (Myongji Univ.) AIST 2 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10	Break Networ 11 IOS logi I-5 I-6 O-9	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr	power transistors Garam Kim (Myongji Univ.) AIST 2 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology occess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10	Break Networ 11 IOS logi I-5 I-6 O-9	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho	power transistors Garam Kim (Myongji Univ.) AIST 2 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology ocess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory Kyung Hee University
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25	Break Networ 11 IOS log I-5 I-6 O-9 O-10	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic	power transistors Garam Kim (Myongji Univ.) AIST 2 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology ocess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory kyung Hee University eat-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25	Break Networ 11 IOS logi I-5 I-6 O-9 O-10	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang	power transistors Garam Kim (Myongji Univ.) AIST 2 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology ocess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory Kyung Hee University
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25 10:40	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40	Break Networ 11 IOS logi I-5 I-6 O-9 O-10 O-11	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang	power transistors Garam Kim (Myongji Univ.) Garam Kim (Myongji Univ.) AIST 22 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology ocess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory kyung Hee University al-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers Seoul National University
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25 10:40 10:55	17:45 19:30 ay, July ON 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15	Break Networ 11 IOS log I-5 I-6 O-9 O-10 O-11 Break	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang	power transistors Garam Kim (Myongji Univ.) Garam Kim (Myongji Univ.) AIST 22 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology ocess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory kyung Hee University al-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers Seoul National University
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25 10:40 10:55 SESSIC	17:45 19:30 ay, July ON 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15	Break Networ 11 OS logi I-5 I-6 O-9 O-10 O-11 Break	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C	Garam Kim (Myongji Univ.) AIST 22 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology occess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory kyung Hee University cal-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers Seoul National University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25 10:40 10:55 SESSIC	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : M co-chain	Break Networ 11 OS logi I-5 I-6 O-9 O-10 O-11 Break IOS logi	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2	Garam Kim (Myongji Univ.) AIST 22 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology occess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory kyung Hee University cal-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers Seoul National University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25 10:40 10:55 SESSIC	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : M	Break Netwol	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwat Md. Hasan Raza Ansari Transistor Architecture Eva	power transistors Garam Kim (Myongji Univ.) [AIST 22 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology occess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University cal-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers [Seoul National University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density n Cho (Myongji Univ.) King Abdullah University of Science and Technology aluation for Standalone and Embedded 1T DRAM
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25 10:40 10:55 SESSIC	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : M co-chain 11:35	Break Networ 11 IOS logi I-5 I-6 0-9 0-10 0-11 Break IOS logi I-7	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C, c and memory devices 2 K. Sakuma (Kioxia), II Hwat Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata	garam Kim (Myongji Univ.) AIST 22 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology cocess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory [kyung Hee University cal-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers [Seoul National University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density n Cho (Myongji Univ.) [King Abdullah University of Science and Technology aluation for Standalone and Embedded 1T DRAM AIST, Keio University
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25 10:40 10:55 SESSIC 11:15	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : M co-chain 11:35	Break Networ 11 IOS logi I-5 I-6 0-9 0-10 0-11 Break IOS logi I-7 0-12	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwan Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H	garam Kim (Myongji Univ.) AIST 22 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology ccess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University ral-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers [Seoul National University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density n Cho (Myongji Univ.) [King Abdullah University of Science and Technology aluation for Standalone and Embedded 1T DRAM [AIST, Keio University rydrogen Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25 10:40 10:55 SESSIC 11:15	17:45 19:30 ay, July ON 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 ON 6 : M co-chain 11:35 11:50	Break Netwol 11 IOS logi I-5 I-6 0-9 0-10 0-11 Break IOS logi I-7 0-12 0-13	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwan Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo	power transistors Garam Kim (Myongji Univ.) AIST 2 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology ocess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory Kyung Hee University cal-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers Seoul National University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density n Cho (Myongji Univ.) King Abdullah University of Science and Technology aluation for Standalone and Embedded 1T DRAM AIST, Keio University Vydrogen Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs Seoul National University
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:30 9:50 10:10 10:25 10:40 10:55 SESSIC 11:15 11:35 11:35	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : M co-chain 11:35 11:35 11:50 12:05	Break Networ 11 I-5 I-6 0-9 0-10 0-11 Break IOS logi I-7 0-12 0-13	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwai Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject	garam Kim (Myongji Univ.) AIST 22 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology occess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University ral-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers [Seoul National University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density n Cho (Myongji Univ.) [King Abdullah University of Science and Technology slaution for Standalone and Embedded 1T DRAM [AIST, Keio University Hydrogen Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25 10:40 10:25 10:40 10:55 SESSIC 11:15 11:35 11:35	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : M co-chain 11:35 11:50 12:05 13:05	Break Networ 11 OS logi I-5 I-6 O-9 O-10 O-10 Break OS logi I-7 O-12 O-12 O-13 Lunch	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwat Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break	power transistors Garam Kim (Myongji Univ.) AIST 2 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology occess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory Kyung Hee University cal-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers Seoul National University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density n Cho (Myongji Univ.) King Abdullah University of Science and Technology aluation for Standalone and Embedded 1T DRAM AIST, Keio University Vydrogen Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs Seoul National University
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25 10:40 10:55 SESSIC 11:55 11:35 11:35 11:35	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : M co-chain 11:35 11:50 12:05 13:05	Break Netwol 11 OS log I-5 I-6 0-9 0-10 0-10 Break OS log I-7 0-12 O-12 O-13 Lunch Poster	MOS technologies for GaN 'king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwat Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge)	power transistors Garam Kim (Myongji Univ.) AIST 2 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology occess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory Kyung Hee University cal-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers Seoul National University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density n Cho (Myongji Univ.) King Abdullah University of Science and Technology aluation for Standalone and Embedded 1T DRAM AIST, Keio University Vydrogen Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs Seoul National University
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:30 9:50 10:10 10:25 10:40 10:25 10:40 10:55 SESSIC 11:15 11:35 11:35 11:50	17:45 19:30 ay, July ON 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 ON 6 : M co-chain 11:35 11:35 11:50 11:50 11:50 11:05 11:05	Break Netwol 11 OS logi I-5 I-6 0-9 0-10 0-10 Break OS logi I-7 0-12 0-12 0-13 Lunch Poster	MOS technologies for GaN 'king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwat Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge)	garam Kim (Myongji Univ.) AIST 22 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology access for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University al-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers [Secul National University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density prindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density prindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density prindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density garation for Standalone and Embedded 1T DRAM AIST, Keio University tydrogen Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs Secul National University ion Programming for TFET-Based Flash Memory
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:30 9:50 10:10 10:25 10:25 10:40 10:25 10:40 10:55 SESSIC 11:50 11:15 11:35 11:50	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : M co-chain 11:35 11:50 12:05 13:05 14:05 co-chain 14:25	Break Networ 11 OS logi I-5 I-6 0-9 0-10 0-11 Break OS logi I-7 0-12 0-13 Lunch Poster Break	MOS technologies for GaN 'king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwat Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge)	power transistors Garam Kim (Myongji Univ.) [AIST 22 as Emerging Memory [Sogang University ext Generation Low-Power Logic Technology [Tokyo Institute of Technology [Garam Kim (Myongji Univ.) [Kyung Hee University occess for the N-doped LaB6/LaBx/Ny Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University cal-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers [Secul National University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density In Cho (Myongji Univ.) [King Abdullah University of Science and Technology aluation for Standalone and Embedded 1T DRAM [AIST, Keio University tydragen Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs [Secul National University ion Programming for TFET-Based Flash Memory
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25 10:25 10:40 10:55 SESSIC 11:15 11:35 11:35 11:35 11:50 12:05 13:05	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : M co-chain 11:35 11:50 12:05 13:05 14:05 co-chain 14:25	Break Networ 11 OS logi I-5 I-6 0-9 0-10 0-11 Break OS logi I-7 0-12 0-13 Lunch Poster Break	MOS technologies for GaN 'king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwat Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T.	power transistors Garam Kim (Myongji Univ.) [AIST 22 as Emerging Memory [Sogang University ext Generation Low-Power Logic Technology [Tokyo Institute of Technology cocess for the N-doped LaB6/LaBx/Ny Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University cal-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers [Secul National University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density in Cho (Myongji Univ.) [King Abdullah University of Science and Technology aluation for Standalone and Embedded 1T DRAM [AIST, Keio University ydrogen Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs [Secul National University ion Programming for TFET-Based Flash Memory
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:30 9:50 10:10 10:25 10:40 10:25 10:40 10:55 SESSIC 11:15 11:35 11:35 11:50 12:05 13:05	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : M co-chain 11:35 11:35 11:50 12:05 13:05 14:05 Co-chain 14:25 DN 7 : O co-chain	Break Netword 11 IOS logi I-5 I-6 0-9 0-10 0-11 Break IOS logi I-7 0-12 0-12 I-7 I-7 Break Poster Freak Poster	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwat Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T. tronics, displays, imagers a T. Hosoi (Kwansei Gakuin U Wataru Yashiro	garam Kim (Myongji Univ.) AIST 2 as Energing Memory Sogang University xt Generation Low-Power Logic Technology Tokyo Institute of Technology cess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory Kyung Hee University cal-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers Secul National University yilndrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density n Cho (Myongji Univ.) [King Abdullah University ydogen Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs Secul National University ion Programming for TFET-Based Flash Memory Futase (Western Digital), J. Heo (Ajou Univ.), S. Kim (Sogang Univ.) nd sensors Univ.) Tohoku Univ.
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25 10:40 10:25 10:40 10:55 SESSIC 11:15 11:35 11:35 11:35 11:35	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : M co-chain 11:35 11:35 11:50 12:05 13:05 14:05 Co-chain 14:25 DN 7 : O co-chain	Break Networ 11 OS logi I-5 I-6 0-9 0-10 0-11 Break OS logi I-7 0-12 0-12 I-7 Break Poster Break ptoelect I-8	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwan Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T. tronics, displays, imagers a T. Hosoi (Kwansei Gakuin U Wataru Yashiro Recent Advances in Synchi	power transistors Garam Kim (Myongji Univ.) AIST 29 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology cocess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University act-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers [Seoul National University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density Indrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density ustation for Standalone and Embedded 1T DRAM AIST, Keio University sydragen Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs [Seoul National University ion Programming for IFET-Based Flash Memory Futase (Western Digital), J. Heo (Ajou Univ.), S. Kim (Sogang Univ.) Aid sensors Univ.), Donghwan Ahn (Kookmin Univ.) Tohoku Univ. Toro X-ray Imaging and Tomography
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:30 9:50 10:10 10:25 10:40 10:25 10:40 10:55 SESSIC 11:15 11:35 11:35 11:35 11:50	17:45 19:30 ay, July N 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 N 6 : M co-chain 11:35 11:50 12:05 13:05 14:05 co-chain 14:25 DN 7 : O co-chain 14:45	Break Networ 11 OS logi I-5 I-6 0-9 0-10 0-11 Break OS logi I-7 0-12 0-12 I-7 Break Poster Break ptoelect I-8	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwa Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T. tronics, displays, imagers a T. Hosoi (Kwansei Gakuin I Wataru Yashiro Recent Advances in Synchi Kyusang Lee	garam Kim (Myongji Univ.) [AIST 2 as Emerging Memory [Sogang University ext Generation Low-Power Logic Technology [Tokyo Institute of Technology cocess for the N-doped LaBG/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University cal-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers [Secul National University val-Channel Charge-Trap-Memory Trin Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers [Secul National University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density In Cho (Myongji Univ.) King Abdullah University Yorgean Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs [Secul National University Yorgean Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs [Secul National University Yorgean Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs [Secul National University Yorgean Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs [Secul National University Ion Programming for TFET-Based Flash Memory
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:30 10:10 10:25 10:40 10:55 SESSIC 11:15 11:35 11:35 11:50 12:05 13:05 13:05	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : M co-chain 11:35 11:50 12:05 13:05 14:05 Co-chain 14:25 DN 7 : O co-chain 14:45	Break Netwol 11 OS logi I-5 I-6 0-9 0-10 0-11 Break OS logi I-7 0-12 0-13 Lunch Poster Break I-73 0-12 0-13 Lunch Poster I-8	MOS technologies for GaN 'king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C, c and memory devices 2 K. Sakuma (Kioxia), II Hwan Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T. tronics, displays, imagers a T. Hosoi (Kwansei Gakuin I Wataru Yashiro Recent Advances in Synchi Kyusang Lee Bio-inspired Neuromorphic	garam Kim (Myongji Univ.) [AIST 28 as Emerging Memory Sogang University 28 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology Tokyo Institute of Technology cess for the N-doped LaBE/LaBENNy Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University al-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers [Secul National University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density validning Univ.) [King Abdullah University ydrogen Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs [Secul National University for TFET-Based Flash Memory Futase (Western Digital), J. Heo (Ajou Univ.), S. Kim (Sogang Univ.) nd sensors Univ.), Donghwan Ahn (Kookmin Univ.) Torboku Univ. Torboku Univ. Torboku Univ. Torboku Univ. Torboku Univ. Sensing: Perception and Cognition towards response
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25 10:40 10:55 SESSIC 11:15 11:35 11:35 11:50 12:05 13:05 14:05	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : M co-chain 11:35 11:50 12:05 13:05 14:05 Co-chain 14:25 DN 7 : O co-chain 14:45 15:05	Break Networ 11 OS logi I-5 I-6 0-9 0-10 0-11 Break 00-11 Break 00-11 Break 00-13 Lunch Poster I-8 I-8	MOS technologies for GaN 'king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwan Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T. tronics, displays, imagers a T. Hosoi (Kwansei Gakuin I Wataru Yashiro Recent Advances in Synchi Kyusang Lee Bio-inspired Neuromorphic Young Hoon Kim	garam Kim (Myongji Univ.) [AIST] 28 as Emerging Memory [Sogang University] ext Generation Low-Power Logic Technology [Tokyo Institute of Technology cess for the N-doped LaBK/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University] al-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers [Secul National University] yindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density in Cho (Myongji Univ.) [King Abdullah University of Science and Technology Judational University yindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density vidrogen Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs [Secul National University] total Performance Futase (Western Digital), J. Heo (Ajou Univ.), S. Kim (Sogang Univ.) nd sensors Univ.), Donghwan Ahn (Kockmin Univ.) [Tohoku Univ.] Sensors Univ.), Donghwan Ahn (Kockmin Univ.) [Tohoku Univ.] Sensors Univ.), Donghwan Ahn (Cognition towards response
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:30 9:50 10:10 10:25 10:40 10:25 10:40 10:55 SESSIC 11:15 11:35 11:50 12:05 13:05 13:05 13:05 14:25	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : M co-chain 11:35 11:50 12:05 13:05 14:05 DN 7 : O co-chain 14:25 DN 7 : O co-chain 14:45 15:05	Break Netwol 11 OS logi I-5 I-6 0-9 0-10 0-11 Break OS logi I-7 0-12 0-13 Lunch Poster Break I-73 0-12 0-13 Lunch Poster I-8 I-9 0-14	MOS technologies for GaN 'king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwat Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T. tronics, displays, imagers a T. Hosoi (Kwansei Gakuin U Wataru Yashiro Recent Advances in Synchi Kyusang Lee Bio-inspired Neuromorphic Young Hoon Kim	gener transistors Garam Kim (Myongji Univ.) [AIST 2 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology [Tokyo Institute of Technology] cocess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University] rad-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IG2O Active and ZnO Charge-Trap Layers [Secul National University] ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density vitrainial University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density vitrainial University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density vitrainial University ylindrical University ylondvinversity of Science and Technology Justito for Standalone and Embedded 11 DRAM [AIST, Keio University ydon Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs Secul National University scena mation University using of TFET-Based Flash Memory Terase (Western Digital), J. Heo (Aj
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:30 9:50 10:10 10:25 10:40 10:25 3ESSIC 11:15 11:35 11:35 11:50 12:05 13:05 13:05 13:05	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : M co-chain 11:35 11:50 12:05 13:05 14:05 Co-chain 14:25 DN 7 : O co-chain 14:45 15:05	Break Netwol 11 IOS logi I-5 I-6 0-9 0-10 0-11 Break I-7 0-12 0-13 Lunch Poster Jtoelect I-8 I-9 0-14	MOS technologies for GaN 'king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertice Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwan Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T. tronics, displays, imagers a T. Hosoi (Kwansei Gakuin U Wataru Yashiro Recent Advances in Synchi Kyusang Lee Bio-inspired Neuromorphic Young Hoon Kim Improved photocurrent-to- Lingrui Li	garam Kim (Myongji Univ.) AIST 2 as Emerging Memory Segarg University Control Contervity Contervity Control Control Control Contrel Con
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:30 9:50 10:10 10:25 10:25 10:40 10:55 SESSIC 11:15 11:35 11:50 11:50 11:50 14:25 13:05 14:25	17:45 19:30 ay, July DN 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : M co-chain 11:35 11:50 13:05 14:05 DN 7 : O co-chain 14:25 DN 7 : O co-chain 14:45 15:05 15:35	Break Networ 11 OS logi I-5 I-6 0-9 0-10 0-110	MOS technologies for GaN 'king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertice Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwan Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T. tronics, displays, imagers a T. Hosoi (Kwansei Gakuin U Wataru Yashiro Recent Advances in Synchi Kyusang Lee Bio-inspired Neuromorphic Young Hoon Kim Improved photocurrent-to- Lingrui Li	gener transistors Garam Kim (Myongji Univ.) [AIST 2 as Emerging Memory Sogang University ext Generation Low-Power Logic Technology [Tokyo Institute of Technology] cocess for the N-doped LaB6/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University] rad-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IG2O Active and ZnO Charge-Trap Layers [Secul National University] ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density vitrainial University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density vitrainial University ylindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density vitrainial University ylindrical University ylondvinversity of Science and Technology Justito for Standalone and Embedded 11 DRAM [AIST, Keio University ydon Annealing Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs Secul National University scena mation University using of TFET-Based Flash Memory Terase (Western Digital), J. Heo (Aj
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25 10:25 10:40 10:55 SESSIC 11:15 11:35 11:35 11:35 11:50 14:05 SESSIC 14:25 14:25 14:25 15:35	17:45 19:30 ay, July ON 5 : M co-chain 9:50 10:10 10:25 10:40 10:55 11:15 ON 6 : M co-chain 11:35 11:50 12:05 13:05 14:05 13:05 14:45 0N 7 : O co-chain 14:45 15:05 15:20	Break Networ 11 OS logi I-5 I-6 0-9 0-10 0-110	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwa Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T. tronics, displays, imagers a T. Hosoi (Kwansei Gakuin U Wataru Yashiro Recent Advances in Synchi Kyusang Lee Bio-inspired Neuromorphic Young Hoon Kim Improved photocurrent-to- Lingrui Li Electron Emission Propertie	gower transistors Garam Kim (Myangji Univ.) AIST 2 as Emerging Memory Segang University access for the N-doped LaB6/LaBAVy Stack Structure to Realize Flaating-gete type Non-volatile Memory [Xyung Hee University access for the N-doped LaB6/LaBAVy Stack Structure to Realize Flaating-gete type Non-volatile Memory [Xyung Hee University access for the N-doped LaB6/LaBAVy Stack Structure to Realize Flaating-gete type Non-volatile Memory [Xyung Hee University access for the N-doped LaB6/LaBAVy Stack Structure to Realize Flaating-gete type Non-volatile Memory [Xyung Hee University access for the N-doped LaB6/LaBAVy Stack Structure to Realize Flaating-gete type Non-volatile Memory [Xyung Hee University access for the N-doped LaB6/LaBAVy Stack Structure to Realize Flaating-gete type Non-volatile Memory [Seoul National University access for the N-doped LaB6/LaBAVy Stack Structure to Realize Flaating-gete type Non-volatile Memory [Seoul National University access for the N-doped LaB6/LaBAVy Stack Structure to Realize Flaating-gete type Non-volatile Memory [Seoul National University access for Standalone and Embedded 17 DRAM [AST, Keio University action for Standalone and Embedded 17 DRAM [AST, Keio University action for Standalone and Embedded 17 DRAM [AST, Keio University action for Standalone and Embedded 17 DRAM [Astrice] National University action Programming for TFET-Based Flash Memory action X-ray Imaging and Tomography [University of Science] [Totase (Western Digital), J. Heo (Ajou Univ.), S. Kim (Segang Univ.) action X-ray Imaging and Tomography [University of Virgina] Sensing: Perception and Cognition towards response [Ajou University action Active Structure Characteristics in AlGeN/GeN-based ultraviolet sensor [Nagaya University action Characteristics in AlGeN/GeN-based ultraviolet sensor [Nagaya University action Characteristics in AlGeN/GeN-based ultraviolet sensor [Nagaya University]
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:30 10:10 10:25 10:25 10:40 10:25 10:40 10:55 10:40 10:55 10:40 10:55 10:40 10:25 10:40 10:25 10:40 10:25 10:40 10:25 10:40 10:25 10:40 10:25 10:40 10:55 10:40 10:55 10:55 10:40 10:55 10:55 10:40 10:55 10:55 10:40 10:55 10:55 10:40 10:55 1	17:45 19:30 ay, July DN 5 : N co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : N co-chain 11:35 11:50 13:05 14:05 Co-chain 14:25 DN 7 : O co-chain 14:25 DN 7 : O co-chain 14:45 15:55 co-chain 15:55 co-chain 15:55	Break Netwol 11 OS logi I-5 I-6 0-9 0-10 0-10 0-11 Break O-11 Break 0-13 Lunch Poster I-7 0-12 0-13 Lunch Poster I-8 I-9 0-14 0-15 Break	MOS technologies for GaN 'king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertice Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwan Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T. tronics, displays, imagers a T. Hosoi (Kwansei Gakuin U Wataru Yashiro Recent Advances in Synchi Kyusang Lee Bio-inspired Neuromorphic Young Hoon Kim Improved photocurrent-to- Lingrui Li	gower transistors Garam Kim (Myangji Univ.) AIST 2 as Emerging Memory Segang University access for the N-doped LaB6/LaBAVy Stack Structure to Realize Floating-gate type Non-volatile Memory [Xyung Hee University access for the N-doped LaB6/LaBAVy Stack Structure to Realize Floating-gate type Non-volatile Memory [Xyung Hee University access for the N-doped LaB6/LaBAVy Stack Structure to Realize Floating-gate type Non-volatile Memory [Xyung Hee University access for the N-doped LaB6/LaBAVy Stack Structure to Realize Floating-gate type Non-volatile Memory [Xyung Hee University access for the N-doped LaB6/LaBAVy Stack Structure to Realize Floating-gate type Non-volatile Memory [Xyung Hee University access for the N-doped LaB6/LaBAVy Stack Structure to Realize Floating-gate type Non-volatile Memory [Seoul National University access for the N-doped LaB6/LaBAVy Stack Structure to Realize Floating-gate type Non-volatile Memory [Seoul National University access for the N-doped LaB6/LaBAVy Stack Structure to Realize Floating-gate type Non-volatile Memory [Seoul National University access for the Improvement of the Program/Erase Efficiency and Memory Density [Seoul National University access for Standalone and Embedded 1D PRAM [AST, Keio University] access for Programming for TFET-Based Float Memory [Seoul National University] action of Standalone and Embedded 1D PRAM [AST, Keio University] access for Programming for TFET-Based Float Memory [Seoul National University] action Scatter Digital), J. Hee (Ajou Univ.), S. Kim (Segang Univ.) action X-ray Imaging and Tomography [University of Virginia] Seouling: Perception and Cognition towards response [Ajou University] action Characetristics in AlGeN/GaN-based ultraviolet sensor [Nagaya University] action Characetristics in AlGeN/GaN-based ultraviolet sensor [Nagaya University] action Characetristics in AlGeN/GaN-based ultraviolet sensor [Nagaya University]
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25 10:25 10:40 10:55 SESSIC 11:15 11:35 11:35 11:35 11:50 14:05 SESSIC 14:25 14:25 14:25 15:35	17:45 19:30 ay, July DN 5 : N co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : N co-chain 11:35 11:50 13:05 14:05 Co-chain 14:25 DN 7 : O co-chain 14:25 DN 7 : O co-chain 14:45 15:55 co-chain 15:55 co-chain 15:55	Break Networ 11 OS logi I-5 I-6 0-9 0-10 0-110	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwa Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T. tronics, displays, imagers a T. Hosoi (Kwansei Gakuin I Wataru Yashiro Recent Advances in Synchi Kyusang Lee Bio-inspired Neuromorphic Young Hoon Kim Improved photocurrent-to- Lingrui Li Electron Emission Propertic T. Mori (AIST), Donghwan Tomohiro Maegawa	garam Kim (Myongji Univ.) [AIST 2 as Emerging Memory Segard University ox Generation Low-Power Logic Technology [Takyo Institute of Technology Cases for the N-doped LaBo/LaBNNy Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University cases for the N-doped LaBo/LaBNNy Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University gal-Channel Charge-Trap-Memory Thin-Flim Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers [Sacaul National University gindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density prindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density prindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density prindrical Vertical INAND Flash Memory King Abdulah University of Science and Technology puscher Anneeling Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs [Sacaul National University for Resors Univ.) Flatase (Western Digital), J. Heo (Ajou Univ.), S. Kim (Sagang Univ.) rd sensors Univ.) Testime Science and Temography
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:50 10:10 10:25 10:25 10:40 10:55 10:55 11:15 11:35 11:35 11:50 14:05 13:05 14:05 14:25 14:25 14:45 15:55	17:45 19:30 ay, July DN 5 : No co-chain 9:50 10:10 10:25 10:40 10:55 11:15 DN 6 : No co-chain 11:35 11:35 11:35 11:50 12:05 13:05 14:25 DN 7 : O co-chain 14:45 15:05 15:55 co-chain 15:55 co-chain 15:155	Break Netwol 11 OS logi I-5 I-6 0-9 0-10 0-10 0-11 Break O-11 Break 0-12 0-13 I-7 0-12 0-13 I-7 0-13 I-7 0-13 I-7 0-13 I-7 0-14 0-15 Break 0-14 I-9 0-14 I-9 I-10	MOS technologies for GaN king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwa Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T. tronics, displays, imagers a T. Hosoi (Kwansei Gakuin I Wataru Yashiro Recent Advances in Synchi Kyusang Lee Bio-inspired Neuromorphic Young Hoon Kim Improved photocurrent-to- Lingrui Li Electron Emission Propertic T. Mori (AIST), Donghwan Tomohiro Maegawa	garam Kim (Myongji Univ.) [AIST 2 as Emerging Memory [Sogang University cccss for the N-dood LaBf/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University ack Generation LaBf/LaBxNy Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University ack Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers [Sooul National University] plindrical Vertical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density n Che (Myongji Univ.) [King Adoullah University] plindrical University plindrical University yundra Annealing Improving the Cryaganic Operation of Si (110)-oriented n-MOSFETs [Seoul National University] yudiga Annealing Improving the Cryaganic Operation of Si (110)-oriented n-MOSFETs [Seoul National University] for Programming for TFET-Based Flash Memory Futase (Western Digital), 1. Heo (Ajou Univ.), S. Kim (Sogang Univ.) net sensors University University University University University University <t< td=""></t<>
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:30 10:10 10:25 10:25 10:40 10:25 10:40 10:25 10:40 10:55 10:55 10:40 10:55 10:40 10:55 10:25 10:40 10:25 10:25 10:40 10:25 10:25 10:40 10:25 10:25 10:40 10:55 10:55 10:40 10:55 1	17:45 19:30 ay, July DN 5 : N co-chain 9:50 10:10 10:25 10:40 10:55 10:40 10:55 11:15 DN 6 : N co-chain 11:35 11:50 12:05 13:05 14:05 14:45 15:55 Co-chain 14:45 15:55 15:55 Co-chain 16:15	Break Netwol 11 OS logi I-5 I-6 0-9 0-10 0-10 0-11 Break OS logi I-7 0-12 0-13 I-7 0-12 I-7 0-13 I-7 0-12 0-13 I-7 0-13 I-7 0-14 0-15 Break 0-14 I-9 0-14 I-9 I-10	MOS technologies for GaN 'king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertice Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwat Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T. tronics, displays, imagers a T. Hosoi (Kwansei Gakuin U Wataru Yashiro Recent Advances in Synchi Kyusang Lee Bio-inspired Neuromorphic Young Hoon Kim Improved photocurrent-to- Lingrui Li Electron Emission Propertie T. Mori (AIST), Donghwan A Application of thermal diod Daewon Lee	geram Kim (Myongji Univ.) [AIST 21 as Emerging Memory Saging University ext Generation Low-Power Logic Technology [Tokyo Institute of Technology ceases for the N-doped LaBG/LaBANy Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University al-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Layers [Secul National University al-Channel Charge-Trap-Memory for the Improvement of the Program/Erase Efficiency and Memory Density vidicial University gend National University yidrogen Annoaling Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs Secul National Information for Cryogenic Operation of Si (110)-oriented n-MOSFETs Secul National Information of Congraphic yidrogen Annoaling Improving the Cryogenic Operation of Si (110)-oriented n-MOSFETs Secul National University forkeut univ.) Techse (Western Digital), J. Hee (Ajau Univ.), S. Kim (Sagang Univ.) retrase (Western Digital), J. Hee (Ajau Univ.), S. Kim (Sagang Univ.) retrase (Western Digital), J. Hee (Ajau Univ.), S. Kim (Sagang Univ.) Techse (Western Digital), J. Hee (Ajau Univ.), S. Kim (Sagang Univ.) Techse (Western Digital), J. Hee (Ajau Univ.), S. Kim (S
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:30 10:10 10:25 10:25 10:40 10:55 10:40 10:55 10:55 11:15 11:50 1	17:45 19:30 ay, July DN 5 : N co-chain 9:50 10:10 10:25 10:40 10:55 10:40 10:55 10:40 10:55 11:15 DN 6 : N co-chain 11:35 11:50 13:05 14:05 13:05 14:05 DN 7 : O co-chain 14:45 DN 7 : O co-chain 14:45 15:55 co-chain 15:35 15:55 co-chain 16:15	Break Networ 11 OS logi I-5 I-6 0-9 0-10 0-11 Break 0-11 Break 0-12 0-13 I-7 0-12 0-13 I-7 0-13 I-8 I-9 0-14 0-15 Break I-10 I-11	MOS technologies for GaN 'king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertice Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwat Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T. tronics, displays, imagers a T. Hosoi (Kwansei Gakuin U Wataru Yashiro Recent Advances in Synchi Kyusang Lee Bio-inspired Neuromorphic Young Hoon Kim Improved photocurrent-to- Lingrui Li Electron Emission Propertie T. Mori (AIST), Donghwan A Application of thermal diod Daewon Lee	gener transistors Gener Kim (Myongii Univ.) [AIST 2a Emerging Memoy Speang University 2a Generation Low-Power Logic Technology [Tokyo Institute of Technology Consers for the N-coole LaBS/LBBNY Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University al-Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and ZnO Charge-Trap Leyers [Secul National University Siceul National University Ying Abdulah University of Science and Technology Incho (Myongii Univ.) [King Abdulah University of Science and Technology Ingra Abdulah University of Science and Technology Ingra Abdulah University of Science and Technology Ingra Abdulah University Information for TET-Based Flash Memory Fitase (Western Digital), J. Heo (Ajou Univ.), S. Kim (Sogang Univ.) Ind sensors Univ.), Donghwan Ahn (Kookmin Univ.) Torba Univ. [Jayu university Jou aniversity University of Virginia Sensors Univ.), Donghwan Ahn (Kookmin Univ.) Torba X-ray Imaging and Tornography University of
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:30 10:10 10:25 10:40 10:25 10:40 10:55 SESSIC 10:40 10:55 10:40 10:55 10:40 10:55 10:40 11:15 11:35 11:50 11:50 14:05 13:05 14:45 14:45 14:45	17:45 19:30 ay, July DN 5 : N co-chain 9:50 10:10 10:25 10:40 10:55 10:40 10:55 10:40 10:55 10:40 10:55 11:15 DN 6 : N co-chain 11:35 11:50 13:05 14:05 13:05 14:25 DN 7 : O co-chain 14:45 15:55 co-chain 15:55 co-chain 16:15 16:35	Break Networ 11 OS logi I-5 I-6 0-9 0-10 0-110 0-110 0-110 0-110 0-112 0-112 0-12 0-13 I-7 0-12 0-13 I-7 0-13 I-7 0-13 I-7 0-13 I-7 0-13 I-7 0-13 I-10 I-10 I-11 I-11	MOS technologies for GaN 'king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwat Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T. tronics, displays, imagers a T. Hosoi (Kwansei Gakuin U Wataru Yashiro Recent Advances in Synchi Kyusang Lee Bio-inspired Neuromorphic Young Hoon Kim Improved photocurrent-to- Lingrui Li Electron Emission Propertid T. Mori (AIST), Donghwan A Application of thermal diod Daewon Lee Fluidic self-assembly trans Yoshiharu Nakajima	Geram Kim (Myongii Univ.) [AST 2 as Emerging Memory [Sogang University St Generation Low-Power Logic Technology [Tokyo Institute of Technology coses for the N-cooled LaBS/LaBS/Ny Stack Structure to Realize Floating-gate type Non-volatile Memory [Kyung Hee University all Channel Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and Zn0 Charge-Trap Layers [Socal National University valid Charge-Trap-Memory Thin-Film Transistors with 60-nm Channel Length by Using IGZO Active and Zn0 Charge-Trap Layers [Socal National University Vigrig Abdulla University Vigrig Abdulla University Vigrig Abdulla University Vigrig Abdulla University Science and Technology Idation for Standalone and Embedded 1T DRAM [AIST, Keiu University Vigrige Annealing Improving the Cryogenic Operation of St (110)-oriented n-MOSPETs [Secal National University Inter-Degramming for TFET-Based Flash Memory Futase (Western Digital), J. Hee (Ajou Univ.), S. Kim (Sogang Univ.) at senses University Vigrinia [University Of Wigninia (Socknini Univ.) [University Vigrinia
16:55 17:25 17:45 Tuesd SESSIC 9:30 9:30 10:10 10:25 10:25 10:55 SESSIC 11:15 11:35 11:35 11:35 11:50 12:05 13:05 14:05 SESSIC 14:25 15:55 16:35 16:35	17:45 19:30 ay, July DN 5 : N co-chain 9:50 10:10 10:25 10:40 10:55 10:40 10:55 10:40 10:55 11:15 DN 6 : N co-chain 11:35 11:50 13:05 14:05 13:05 14:05 DN 7 : O co-chain 14:45 DN 7 : O co-chain 14:45 15:55 co-chain 15:35 15:55 co-chain 16:15	Break Netwol 11 OS logi I-5 I-5 I-6 0-9 0-10 0-10 0-11 Break 0-12 0-13 I-7 0-12 0-13 I-7 0-13 I-7 0-13 I-7 0-13 I-7 0-14 0-15 Break 1-9 0-14 I-8 I-9 0-14 I-10 I-11 I-12 I-12 I-12	MOS technologies for GaN 'king Session (Lounge) c and memory devices 1 H. Ikeda (Shizuoka Univ.), Shinji Migita Status of Ferroelectric HfO Sihyun Kim Ferroelectric Devices as Ne Eun-Ki Hong Development of Etching Pr Yun-Ju Cho Scaling Feasibility of Vertic Jin Ho Chang Recessed Channel Hemi-C c and memory devices 2 K. Sakuma (Kioxia), II Hwat Md. Hasan Raza Ansari Transistor Architecture Eva Shunsuke Shitakata Additional High-Pressure H Jae Seung Woo Effective Hot Carrier Inject break Session (Lounge) T. Suwa (Tohoku Univ.), T. tronics, displays, imagers a T. Hosoi (Kwansei Gakuin U Wataru Yashiro Recent Advances in Synchi Kyusang Lee Bio-inspired Neuromorphic Young Hoon Kim Improved photocurrent-to- Lingrui Li Electron Emission Propertid T. Mori (AIST), Donghwan A Application of thermal diod Daewon Lee Fluidic self-assembly trans Yoshiharu Nakajima	garam Kim (Myongi Univ.) [AST 2 as Emerging Memory 3 garge University extra Kim (Myongi Univ.) [ANT 2 as Emerging Memory 3 garge University extra Kim (Above LaBpC Eachnology [Tokyo Institute of Technology coses for the N-coole LaBpC LaBkNy Stack Structure to Realize Floating-gate type Non-volatile Memory [Xyung Hea University al Channel Charge-Trap-Memory Thin-Film Transistors with 50-nm Channel Length by Using IGZO Active and ZnO Charge Trap Layers [Soci National University yIndrical Varitical NAND Flash Memory for the Improvement of the Program/Erase Efficiency and Memory Density In Cha (Myongi) Univ.) [King Abdulah University [AST, Keio University [Jast] Keio University [Jastresity] University [J