The IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences announces a forthcoming Special Section on VLSI Design and CAD Algorithms to be published in March 2025.

The objective of the special section is to discuss new theoretical or practical developments and techniques in VLSI design and CAD algorithms. The special section solicits paper submission from anyone in this field, and especially from people who present papers at ASP-DAC 2024 and SASIMI 2024. The authors working in this area are strongly encouraged to submit original research papers on the topics which include, but are not limited to, the following areas:

- VLSI design methodology
- Logic synthesis
- Simulations (device, process, circuit, logic, high-level, etc.)
- Physical Design
- Emerging Technologies (Optical circuit design, Quantum computing, Hardware security etc.)
- VLSI architecture
- Low power design
- Analog circuit design
- Co-design
- Test pattern generation
- Cell/module design
- High-level synthesis
- Formal verification
- Layout verification
- System level design
- Design for testability
- Simulation (device, process, circuit, logic, high-level, etc.)
- Test pattern generation
- Design for testability
- Physical Design
- Analog circuit design
- Emerging Technologies (Optical circuit design, Quantum computing, Hardware security etc.)

**Notes for Authors:**

All manuscripts should be prepared according to the “Information for Authors” which is available in [https://www.ieice.org/eng/shiori/mokuji_ess.html](https://www.ieice.org/eng/shiori/mokuji_ess.html). The standard number of pages is 8 for a PAPER and 2 for a LETTER.

For the initial submission of a LETTER, the number of pages excluding References is at most 4.

This special section will accept papers only by electronic submission. Prospective authors are requested to follow carefully the submission process described below.

- Submit a complete paper and electronic files (Word/TeX files, figures, authors’ photos and biography) for publishing using the IEICE Web site [https://review.ieice.org/regist/regist_baseinfo_e.aspx](https://review.ieice.org/regist/regist_baseinfo_e.aspx). Authors should choose the “[Special-VL] VLSI Design and CAD Algorithms” as a “Journal/Section” on the online screen. Do not choose “[Regular-EA]”. See details on [https://www.ieice.org/eng/shiori/mokuji_ess.html](https://www.ieice.org/eng/shiori/mokuji_ess.html).

The manuscript will undergo the standard review process of the IEICE Transactions on Fundamentals.

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**Deadline of Submission:**

March 8, 2024

**Further Information:**

Prof. Shimpei Sato (Shinshu Univ.)
Department of Electrical and Computer Engineering, Shinshu University
E-mail: satos@shinshu-u.ac.jp

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