Call for Papers

-------- Special Section on Multiple-Valued Logic and VLSI Computing --------

The IEICE Transactions on Information and Systems announces that it will publish a special section entitled “Special Section on Multiple-Valued Logic and VLSI Computing” in August 2024.

Recent development of System-on-Chip (SoC) technology has been accelerated by device scaling which drives improved performance and power, high functionality and cost reduction. However, there occur unprecedented serious problems today at very small device feature sizes. To solve the problems, innovative new-concept VLSI computing technology such as multiple-valued VLSI computing is strongly expected to be developed. Also, logic design based on a multiple-valued concept, multiple-valued algebra and soft computing are expected to be effectively employed for the next-generation digital computing and artificial intelligent applications. From this point of view, we have planned Special Section on Multiple-Valued Logic and VLSI Computing to be published in August 2024. To discuss the same frontier area, the 53rd IEEE International Symposium on Multiple-Valued Logic (ISMVL2023) was held in May 2023 in Shimane, Japan. We solicit for submission of the papers on multiple-valued logic and VLSI computing, not limited to the presented papers in the ISMVL2023. We welcome demonstration of the recent development of novel and new-concept computing technology.

1. Scope
This special section aims at timely dissemination of research in these areas. Possible topics include, but are not limited to:

- Multiple-Valued Algebra & Logic
- Fuzzy Logic
- Soft Computing
- Quantum Computing
- Logic Design & Switching Theory
- Test & Verification
- Spectrum Technique
- New-Concept VLSI Architecture
- Multiple-Valued logic applications to Big data/Data mining
- Multiple-Valued VLSI Computing
- Nanodevice

2. Submission Instructions
- A manuscript should be prepared according to the guideline given in “The Information for Authors” (https://www.ieice.org/eng/shiori/mokuji_iss.html). We encourage the authors to use the IEICE Style File (https://www.ieice.org/ftp/index-e.html). The preferred length of the manuscript is 8 pages for a PAPER and 2 pages for a LETTER with the format determined by the IEICE Style File.
- Submit the manuscript through the IEICE Web site (https://review.ieice.org/regist/regist_baseinfo_e.aspx). Choose “[Special-LO] Multiple-Valued Logic and VLSI Computing” in the menu of “Journal/Section” in the submission page. Do not choose “[Regular-ED] Information and Systems” or other special sections.
- Authors must agree to the “Copyright Transfer, Article Processing Charge Agreement, Notices from the IEICE, and Privacy Policy” via electronic submission.
- Submission deadline of the manuscript is Oct. 27 2023. (Extended!)

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* Upon accepted for publication, all authors, including authors of invited papers, should pay the article processing charge covering partial cost of publication around April 2024. If payment is not completed by 15 May, 2024 your manuscript will be handled as rejection.

* The standard period of 60 days between the notification (of conditional accept) and the second submission can be shortened according as the review schedule.

* If there are non-members among the authors, we recommend that the authors take this opportunity to join the IEICE. For detailed information on the IEICE Membership Application, please visit the web-page, https://www.ieice.org/eng/r/join/individual_member.html. If all authors are non-members, the article processing charge for non-members will be applied, except for invited papers.

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