The IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences announces a forthcoming Special Section on VLSI Design and CAD Algorithms to be published in March 2024.

The objective of the special section is to discuss new theoretical or practical developments and techniques in VLSI design and CAD algorithms. The special section solicits paper submission from anyone in this field, and especially from people who present papers at ASP-DAC 2023. The authors working in this area are strongly encouraged to submit original research papers on the topics which include, but are not limited to, the following areas:

- VLSI design methodology
- VLSI architecture
- Logic synthesis
- A low power design
- Simulation (device, process, circuit, logic, high-level, etc.)
- Test pattern generation
- Co-design
- Formal verification
- High-level synthesis
- Layout verification
- Floor-planning and placement
- Routing
- Analog circuit design
- System level design
- Low power design
- Cell/module design
- System level design
- Design for testability
- Test pattern generation
- Simulation (device, process, circuit, logic, high-level, etc.)
- Design for testability
- Floor-planning and placement
- System level design
- Test pattern generation
- Simulation (device, process, circuit, logic, high-level, etc.)
- Design for testability
- Floor-planning and placement
- System level design
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- Design for testability
- Floor-planning and placement
- System level design
- Test pattern generation
- Simulation (device, process, circuit, logic, high-level, etc.)
- Design for testability

Notes for Authors:

All manuscripts should be prepared according to the “Information for Authors” which is available at https://www.ieice.org/eng/shiori/mokuji_ess.html. The standard number of pages is 8 for a PAPER and 2 for a LETTER. For the initial submission of a LETTER, the number of pages excluding References is at most 4.

This special section will accept papers only by electronic submission. Prospective authors are requested to follow carefully the submission process described below.

- Submit a complete paper and electronic files (Word/TeX files, figures, authors’ photos and biography) for publishing using the IEICE Web site https://review.ieice.org/regist/regist_baseinfo_e.aspx. Authors should choose the “[Special-VL] VLSI Design and CAD Algorithms” as a “Journal/Section” on the online screen. Do not choose “[Regular-EA]”. See details on https://www.ieice.org/eng/shiori/mokuji_ess.html.

The manuscript will undergo the standard review process of the IEICE Transactions on Fundamentals.

* Authors must agree to the "Copyright Transfer, Article Processing Charge Agreement, Notices from the IEICE, and Privacy Policy" via electronic submission.

Deadline of Submission:

March 10, 2023

Further Information:

Prof. Shimpei Sato
Department of Electrical and Computer Engineering, Shinshu University
Phone: +81-26-269-5472 E-mail: satos@shinshu-u.ac.jp

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