Call for Papers

Special Section on Analog Circuits and Their Application Technologies

The IEICE Transactions on Electronics announces a forthcoming Special Section on Analog Circuits and Their Application Technologies to be published in **October 2023**.

The rapid progress of IoT, AI, 5G and quantum computer demands the evolution of integrated circuits in the fields such as wireless/wireline communication, sensing systems, signal processing, power management and cryo-CMOS, where analog circuits have been playing a crucial role. Analog circuits with high performance and enhanced functionality as well as low power and low cost are challenging to design but strongly demanded for next-generation applications. In addition to pure analog techniques, the scope of this special section includes fundamental issues such as co-design of analog/digital circuits, analog circuits in SoCs, analog circuit design for manufacturability (DFM) and testability (DFT), device modeling techniques, and hardware security. Also, the papers without either chip implementation or measurement results are welcome.

Authors working in this area are invited to submit original research papers on topics, which include, but are not limited to:

- Circuit techniques for wireless/wired/optical communication systems
- RF circuits and broadband circuits
- Low-power/low-voltage circuits
- High-speed/high-precision ADCs and DACs
- Amplifiers, oscillators, PLLs, voltage references, and power management circuits
- Analog/RF integration techniques for SoCs
- Assembly related topics (electronic packaging, SiP, module, EMC, supply noise, ground noise, digital noise, etc.)
- Mixed-signal integration applications (RFID, storage devices, tuners, automotive, sensor and MEMS interfaces, biomedicine and healthcare, etc.)
- Analog techniques for high performance (high frequency ESD structures, power supply circuits, etc.)
- Device modeling techniques
- Device technologies for analog circuits (CMOS, BiCMOS, compound semiconductor, MEMS, etc.)
- Design for manufacturability (DFM) and/or testability (DFT) of analog circuits
- Hardware security

Theoretical papers which do not include chip implementation and its measurement results are also welcome.
Submission due date is extended to November 4, 2022. This special section will accept only PAPERs and BRIEF PAPERs by electronic submission. Prospective authors are requested to carefully follow the submission process described below.
Submit a paper using the IEICE Web site **https://review.ieice.org/regist/regist_baseinfo_e.aspx**. Authors should choose the [Special-TC] Analog Circuits and Related Technologies as the "Journal/ Section" on the online screen. Do not choose [Regular-EC].

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It is recommended that PAPER be within eight pages in length. The maximum number of pages for the initial submission of a BRIEF PAPER must be 4. Manuscripts should be prepared according to the "Information for Authors," the latest version of which is available at: **https://www.ieice.org/eng/shiori/mokuji_es.html**.

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