Call for Papers

------- Special Section on Multiple-Valued Logic and VLSI Computing -------

The IEICE Transactions on Information and Systems announces that it will publish a special section entitled “Special Section on Communication Quality” in August 2021.

Recent development of System-on-Chip (SoC) technology has been accelerated by device scaling which drives improved performance and power, high functionality and cost reduction. However, there occur unprecedented serious problems today at very small device feature sizes. To solve the problems, innovative new-concept VLSI computing technology such as multiple-valued VLSI computing is strongly expected to be developed. Also, logic design based on a multiple-valued concept, multiple-valued algebra and soft computing are expected to be effectively employed for the next-generation digital computing and artificial intelligent applications. From this point of view, we have planned Special Section on Multiple-Valued Logic and VLSI Computing to be published in August 2021. To discuss the same frontier area, the 50th IEEE International Symposium on Multiple-Valued Logic (ISMVL2020) was held in May 2020 in Miyazaki, Japan. We solicit for submission of the papers on multiple-valued logic and VLSI computing, not limited to the presented papers in the ISMVL2020. We welcome demonstration of the recent development of novel and new-concept computing technology.

1. Scope
This special section aims at timely dissemination of research in these areas. Possible topics include, but are not limited to:

- Multiple-Valued Algebra & Logic
- Fuzzy Logic
- Soft Computing
- Quantum Computing
- Logic Design & Switching Theory
- Test & Verification
- Multiple-Valued VLSI Computing
- Spectrum Technique
- New Memory-Based Architecture
- Multiple-Valued logic applications to Big data/Data mining
- Nanodevice
- Soft computing applications to Intelligent Medical and Welfare Engineering
- New-Concept VLSI Architecture
- Applications to Security

2. Submission Instructions
- A manuscript should be prepared according to the guideline given in “The Information for Authors” (https://www.ieice.org/eng/shiori/mokuji_iss.html). We encourage the authors to use the IEICE Style File (https://www.ieice.org/ftp/index-e.html). The preferred length of the manuscript is 8 pages for a PAPER and 2 pages for a LETTER with the format determined by the IEICE Style File.
- Submit the manuscript through the IEICE Web site (https://review.ieice.org/regist/regist_baseinfo_e.aspx). Choose “[Special-LO] Multiple-Valued Logic and VLSI Computing” in the menu of “Journal/Section” in the submission page. Do not choose “[Regular-ED] Information and Systems” or other special sections.
- Authors must agree to the “Copyright Transfer and Page Charge Agreement” via electronic submission.
- Submission deadline of the manuscript is Aug. 28 2018.

Contact:
Shinobu Nagayama  (Dept. of Computer and Network Engineering, Hiroshima City University)
Tel: +81-82-830-1599,   Email: s_naga@hiroshima-cu.ac.jp

3. Special Section Editorial Committee
Guest Editor-in-Chief: Yutaka Hata (Univ. of Hyogo)
Guest Associate Editor-in-Chief: Kazuya Tanigawa (Hiroshima City Univ.), Shinobu Nagayama (Hiroshima City Univ.)
Guest Associate Editors:
Tomoyuki Araki (Hiroshima Inst. of Tech.), Takashi Hiyama (Iwate Univ.), Naofumi Homma (Tohoku Univ.), Yukihiro Iguchi (Meiji Univ.), Naotake Kamiura (Univ. of Hyogo), Mayuka F. Kawaguchi (Hokkaido Univ.), Syoji Kobashi (Univ. of Hyogo), Masanori Natsui (Tohoku Univ.), Tsutomu Sasao (Meiji Univ.), Noboru Takagi (Toyama Pref. Univ.), Koichi Tanno (Univ. of Miyazaki), Yasushi Yuminaka (Gunma Univ.), Takao Waho (Sophia Univ.)

* Upon accepted for publication, all authors, including authors of invited papers, should pay the page charges covering partial cost of publication around April 2021. If payment is not completed by May 15, 2021 your manuscript will be handled as rejection.

* At least one of the authors must be an IEICE member when the manuscript is submitted for review. Invited papers are an exception. We recommend authors unaffiliated with IEICE to apply for the membership (https://www.ieice.org/eng/join/member.html).

* Open Access Publishing: Since January 2017, all papers of the IEICE Transactions on Information and Systems stored in J-STAGE that include all papers published from January 2017 have been opened to all reader in the world through J-STAGE. Open Access Option for many transactions in IEICE will not be applied to papers in January 2020 issue and following issues of the IEICE Transactions on Information and Systems. (Open Access Publishing will be continued after January 2020.). For details on Open Access Publishing and Open Access Options, please carefully refer to “The Information for Authors” (https://www.ieice.org/eng/shiori/mokuji_iss.html). Note that these rules may be changed without notice.