

60 GHz On-Chip Loop Antenna Integrated in a 0.18 μm CMOS Technology

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Abstract- This paper describes the electromagnetic (EM) field analysis of a 60 GHz on-chip loop antenna integrated in a 0.18 μm CMOS Technology. The simulation was compared with the measurement. The reflection coefficient showed good agreement between simulation and measurement by assuming a conductive layer of about 1 μm in the simulation. The radiation efficiency is calculated and it was found that the radiation efficiency can be improved by reducing conductivity of the silicon substrate. The radiation efficiency of 82.6% can be achieved if conductivity is less than 0.1 S/m.

Index terms- On-chip loop antenna, Millimeter-wave, CMOS substrate, Conductive layer, Electromagnetic simulation

I. INTRODUCTION

The CMOS technology can be applied to chips for wireless systems in the 60-GHz band [1]. Recently, in order to integrate the antenna with low cost single chip and CMOS RF front-end circuitry, on-chip antennas have been studied by many researchers [2]. It is important to reduce a connection loss between the CMOS chip and the antenna. The authors have simulated a dipole antenna on the Si CMOS substrate and confirmed good agreement between simulation and measurement by assuming a conductive layer on the surface of the Si CMOS substrate [3].

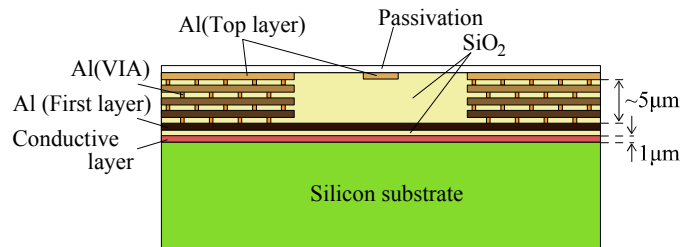
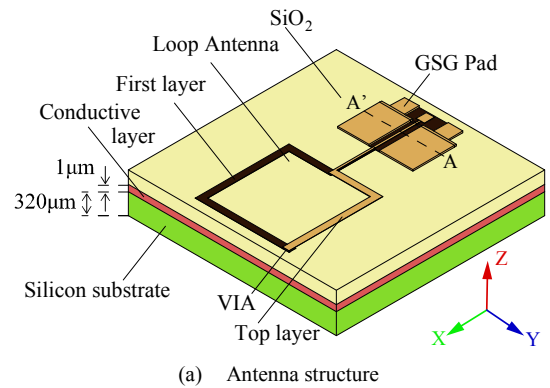
In this paper, an on-chip loop antenna is simulated considering the conductive layer. Simulation result is compared with measurement. The effect of the conductivity of the Si CMOS substrate on the radiation efficiency is investigated.

II. STRUCTURE OF LOOP ANTENNA

Figure 1 shows the structure of the on-chip loop antenna. The size of a silicon chip is 5 mm square and the thickness of silicon substrate is 320 μm . The relative permittivity and conductivity of the silicon substrate are 11.9 and 6300 S/m, respectively. The metal is aluminum and space is filled with SiO_2 insulator. The conductivity of the conductive layer is 10^5 S/m with the thickness of about 1 μm [3]. A passivation layer is on the top surface of the chip. Figure 2 (a) shows the

micrograph of the fabricated on-chip loop antenna. The loop antenna consists of the top metal layer and first metal layer which are connected by vias at the upper left corner in the figure. The loop antenna is fed by the microstrip line and the microstrip line is connected to a GSG pad for 100 μm -pitch GSG probe.

Figure 2 (b) shows the analysis model. Figure 3 shows the 3-D model and the radiation boundary in HFSS. The finite element method (FEM) based EM simulator, Ansoft HFSS, is used for simulation. A vacuum radiation box size is 10mm \times 10mm \times 5mm. The two lumped ports between signal and ground pad in the GSG pad with 100 Ω internal impedance are used for excitation modeling. The reflection coefficient is obtained by converting the 2 \times 2 S-matrix of the two lumped ports [4].



(b) Cross-sectional view (A-A' in (a))

Figure 1: Structure of the on-chip loop antenna

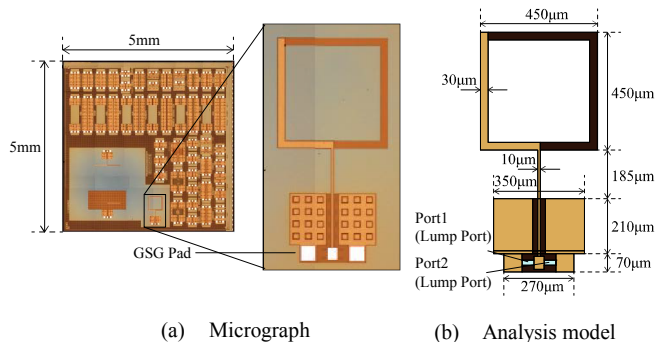


Figure 2: On-chip loop antenna on a silicon CMOS substrate

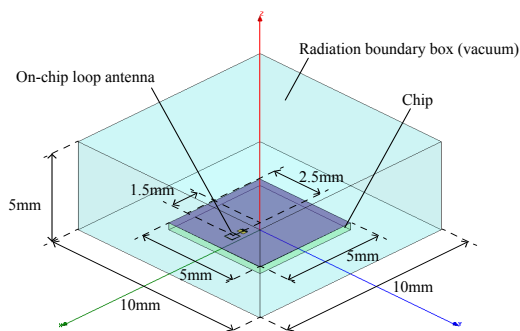


Figure 3: The 3-D model with the radiation boundary box in HFSS

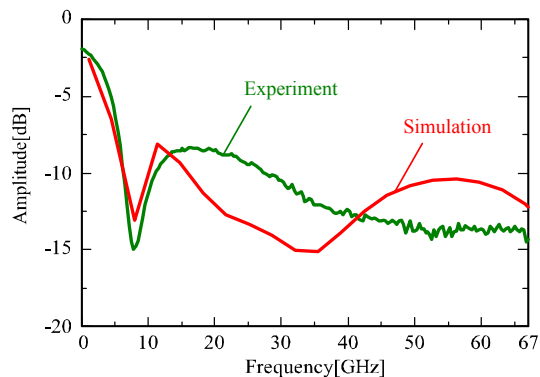
III. RESULTS

Figure 4 shows the frequency characteristics of the reflection coefficient. The reflection coefficient is in good agreement between simulation and measurement by assuming a conductive layer.

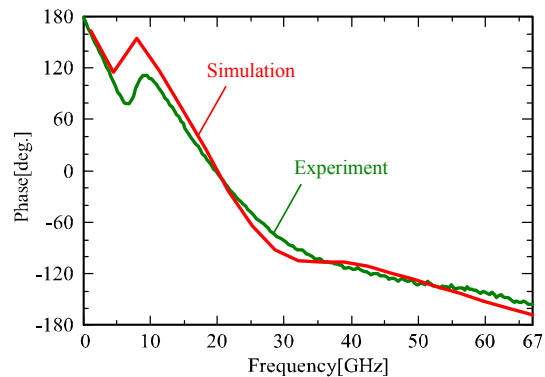
The conductivity of Si CMOS substrate is changed from 10^{-2} S/m to 10^6 S/m at 60 GHz, and the peak gain and the radiation efficiency of the on-chip loop antenna are shown in Figure 5. The radiation efficiency and the peak gain increase as the conductivity of the Si CMOS substrate decreases. The radiation efficiency is 0.021% and the peak gain is -31.2 dBi when the conductivity is 6300 S/m.(a) And the radiation efficiency and the peak gain are saturated to be 82.6% and 6.11 dBi when the conductivity is 0.1 S/m.(b) The residual loss is due to the finite conductivity of metal. Figure 6 shows the 3D radiation patterns when the conductivity is 6300 S/m and 0.1 S/m. They have almost the same patterns, though the gain difference is more than 35dBi.

IV. CONCLUSION

The on-chip loop antenna has been simulated by the EM simulator. The reflection coefficient showed good agreement between simulation and measurement by assuming a conductive layer with the high conductivity on the Si CMOS



(a) Amplitude



(b) Phase

Figure 4: Frequency characteristic of reflection coefficient

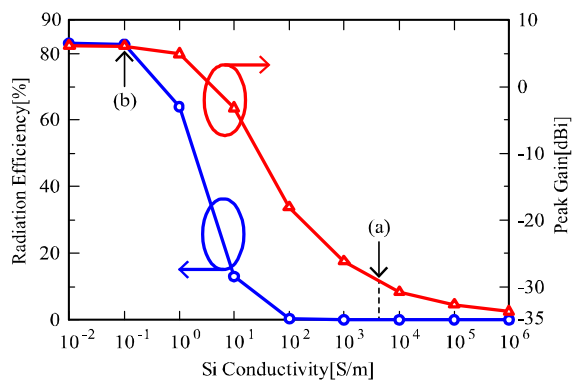
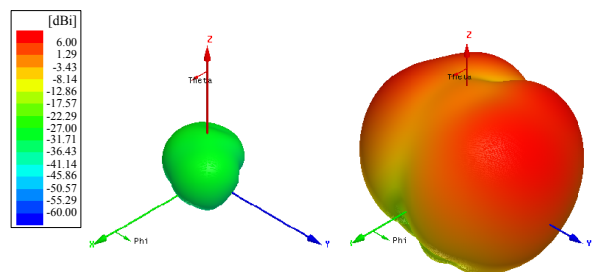


Figure 5: Radiation pattern and gain



(a) Si Conductivity:6300 S/m (b) Si Conductivity:0.1 S/m

Figure 6: Gain pattern (@60 GHz)

substrate surface. The gain and the radiation efficiency can be improved by reducing the conductivity of Si CMOS substrate.

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