Transmission Characteristics of Via Holes in High-Speed PCB

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***Abstract*-A method of analyzing transmission characteristics of via holes in the time domain is presented in this paper. A suitable analysis model is set up using CST (Computer Simulation Technology). With theoretical analysis, the effect of via structures on signal transmission characteristics could be acquired. The simulation results show that appropriate design for via holes can reduce transmission characteristics issues effectively.**

I. INTRODUCTION

As operating frequency and data rate increase, PCB(Printed Circuit Board) layout becomes increasingly dense. The via hole provides a good choice to high-speed multi-layered PCB. However, a discontinuity occurs as a result of the via hole, which is also the cause of some signal integrity problems[1-2], such as time delay, signal reflection and crosstalk. For high-speed PCB, signal integrity is as important as the circuit function and clock rate[3]. Hence, appropriate analysis of electrical characteristics and parasitic parameters of via holes are needed. Several types of via holes and their scattering parameters (S-Parameters) is discussed in [4]. Effects of the structure of via holes on scattering parameters and transmission loss is given in [5]-[6]. All the papers mentioned above are based on the frequency-domain which is less direct than the time-domain. Even though we could achieve transmission characteristics of via holes using TDR in practical problems, there are few papers which disscussed transmission characteristics of via holes using simulation software directly in the time-domain. The one-via hole model and three-via hole model are given in detail in this paper using the time-domain simulation software-CST. And, the transmission characteristics of via holes are studied.

II. VIA HOLE

Via holes[7] are the common holes interconnecting transmission lines on different layers in two-layer or multi-layer PCB. A typical structure of a via hole is shown in Fig. 1.

As operating frequency increases, the parasitic parameters of each via hole should be considered, including parasitic capacitance and parasitic inductance. A typical equivalent circuit of a via hole is shown in Fig. 2.

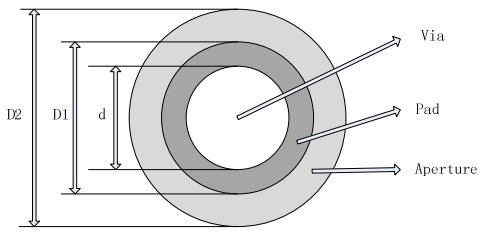


Fig. 1. Via structure. D2 is the aperture diameter, D1 is the pad diameter, d is the via diameter.

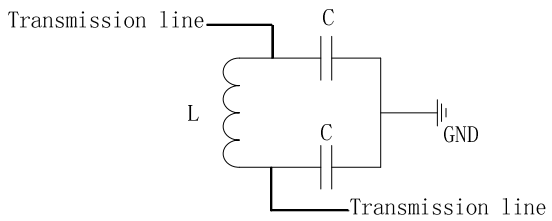


Fig. 2. Equivalent circuit. C is parasitic capacitance, L is the parasitic inductance.

A. Parasitic Capacitance of Via Holes

Parasitic capacitance of a via hole[7] is defined as

$$C = \frac{1.41\varepsilon_r T D_1}{D_2 - D_1} \tag{1}$$

where ε_r is the dielectric constant, and T is the thickness of the PCB.

B. Parasitic Inductance of Via Holes

While there is parasitic capacitance of via holes, there is parasitic inductance. Parasitic inductance of a via hole[7] is defined as

$$L = 5.08h\left[\ln\left(\frac{4h}{d}\right)+1\right] \tag{2}$$

where h is the height of via hole

III. EFFECT OF VIA HOLES ON TIME DELAY

A. Theoretical Analysis

A via hole inevitably puts influence on signal transimission characteristics in high-speed PCB. It could be considered as a transimission line. Its parasitic capacitance increases signal rising time and slows down circuit speed, leading to propagation delay. For instance, the parasitic capacitance of a PCB is 0.23pF from Equation (1), of which the thickness of the substrate is 24mil, the via diameter is 10mil, the pad diameter is 22mil, the aperture diameter is 36mil and the relative dielectric constant of the substrate is 4.3.

For a transmission line of characteristic impedance of $50\,\Omega$, the variation of the rising time caused by the parasitic capacitance is defined as

$$\Delta T_{10\%-90\%} = 2.2C(Z_0/2) = 13\,ps \tag{3}$$

The time delay of one via hole is not notable. However, if numerous via holes are used in the design, the signal quality

will not be guaranteed. Therefore, issues produced by considerable via holes should be taken into account.

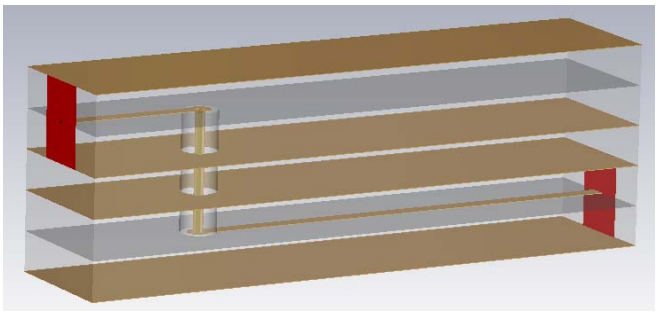
As shown by Equation (1), in order to minimize the time delay, the size of via holes must be carefully studied. The parasitic capacitance is proportional to the via diameter and the thickness of the substrate, and inversely proportional to the aperture diameter. If dielectric materials are given, the via diameter should be minimized and the aperture diameter should be maximized if possible.

Materials and thickness of the substrate definitely have influence on the transmission characteristics of via holes. However, if materials or thickness of the substrate is changed merely, the characteristic impedance of the stripline will deviate from $50\,\Omega$. If so, this comparison will not based on the same conditions. Thus, this paper does its research on condition that materials and thickness of the substrate are seclected.

B. Simulation Analysis

This paper develops a PCB in the CST MICROWAVE STUDIO, as shown in the Fig. 3(a). Input and output of the model are simulated in CST DESIGN STUDIO.

The model is a six-layered PCB where the via diameter is d=10mil, the pad diameter is D1=22mil, the aperture diameter is D2=36mil, the thickness of each layer is h=8mil, the width of the transmission line is 6.8mil and the thickness of copper layer is 0.7mil. The simulation result of this one-via hole is shown in Fig. 3(b).



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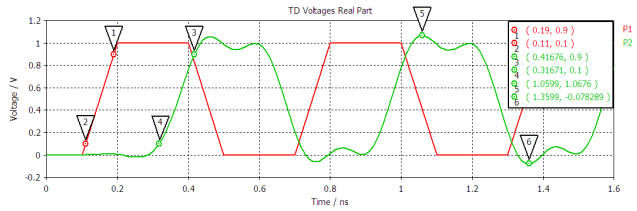
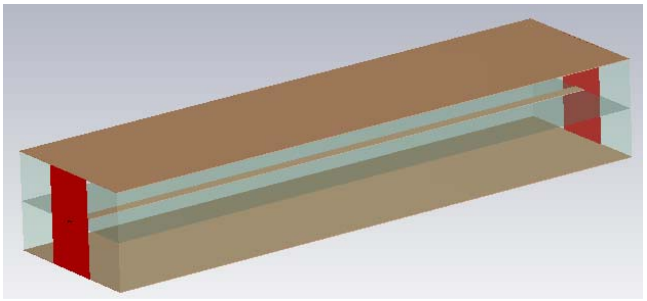


(b)

Fig. 3. One-via hole

In high frequency, the time delay is determined by materials of the substrate and the length of the transmission line. For the transmission line itself has time delay, the time delay of the single stripline should be studied so as to find out the results of the via holes caused. The whole length of the stripline contains the length of the via hole and the original stripline. The model and the result of the time delay are shown in Fig. 4(b).



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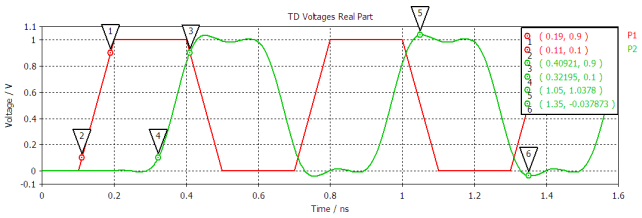
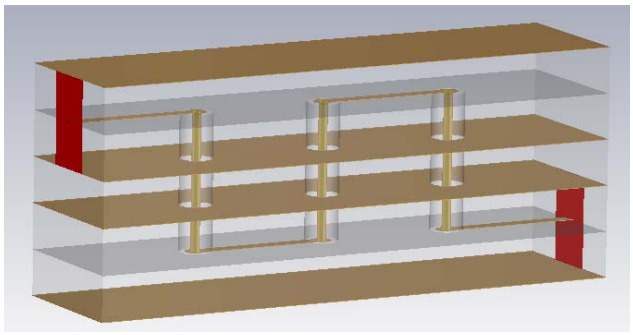


(b)

Fig. 4. Single transmission line

Fig. 3 and 4 showed the rising time $T_{10\%\text{-}90\%}$ of the excitation is 80ps and the rising time $T_{10\%\text{-}90\%}$ of the one-via hole model is 88ps. Then the change $\Delta T_{10\%\text{-}90\%}$ of the rising time caused by the single via hole is 12ps. From Equation (1) and (3), the change of the rising time caused by the single via hole is 13ps. The results of simulation are consistent with that of theoretical analysis.



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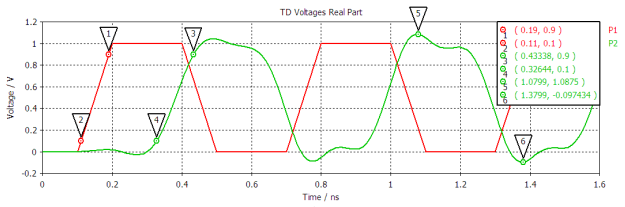


(b)

Fig. 5. Three-via hole

As shown in Figure 5, through modeling and simulating the three-via hole, the rising time of this three-via hole is achieved. The rising time is 107ps. Compared with the module with one-via hole, the time delay of the rising time increases.

Fig. 3, 4 and 5 give the time delay of the input and output at 0.1V. Due to transmission-line effect, the time delay of the

single transmission line is 8ps. However , the time delay of the one-via hole is 20ps and the time delay of the three-via hole is 27ps. As the number of via holes increases, the time delay increases.

When the via diameter is 10mil, the aperture diameter is 36mil and the pad diameter is 18mil, 22mil and 26mil, results of the time delay are shown in Fig. 6.

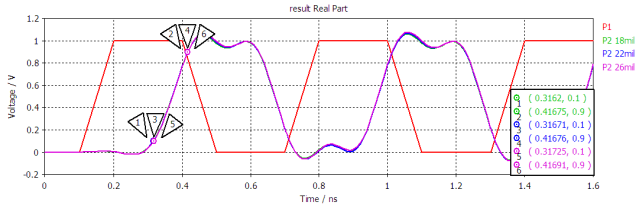


Fig. 6. Different pad diameters

When the via diameter is 10mil, the pad diameter is 22mil and the aperture diameter is 32mil, 36mil and 40mil, results of the time delay are shown in Fig. 7.

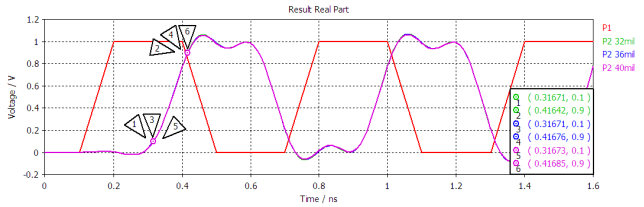


Figure 7 different aperture diameters

As shown in Fig. 6 and 7, the time delay decreases with the increase of via diameter and increases with the increase of aperture diameter. As a result of the combined effect of the complexity of the system and the parasitic parameters, these structures result in time delay indistinctively. But it did happen. From next session, effects caused by the parasitic capacitance is less significant than that caused by the parasitic inductance.

IV. Effect of Via Holes on Signal Reflection

A. Theoretical Analysis

During signal transmitting process, signal feels transient impedance at all times. If the transient impedance is constant, signal propagation will proceed normally; if the transient impedance varies anywhere, signal reflection will happen. Via holes are discontinuities of the transmission line in high frequency and high-speed circuits. The reflection formula[8] is shown by

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{V_{\mathrm{Re}\,flected}}{V_{Incident}} \tag{4}$$

where Γ is reflection coefficient, Z_0 is characteristic impedance, Z_L is transient impedance, $V_{Reflected}$ is reflected voltage, $V_{Incident}$ is incident voltage.

In high-speed PCB, harm caused by the parasitic inductance of via holes is bigger than that of the parasitic capacitance. The parasitic inductance spoils the effectiveness that shunt capacitors and decoupling capacititors have, thus impairing the filtering effect of the whole system. Still using the example above, the parasitic inductance of this via hole is

$$L=0.29\mathrm{nH} \tag{5}$$

If the signal rising time is 0.1ns, the equivalent impedance could be illustrated as follows

$$X_L=\pi L/(T_{10\%-90\%})=9.86\,\Omega \tag{6}$$

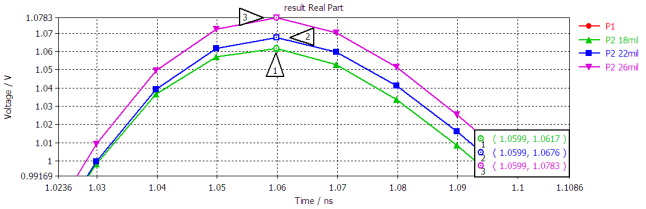
The change in impedance is $9.86\,\Omega$. At this point the reflection coefficient is $\Gamma=0.09$. The bigger change in impedance is, the more reflected signal is. In high frequency, this impedance could not be ignored.

Meanwhile, the signal is reflected when it arrive at the via hole as a result of the parasitic capacitance.

B. Simulation Analysis

As shown in Fig. 3, 4 and 5, the overshoot of the single stripline changes by 3.78% and undershoot by 3.79%. The overshoot of one-via hole changes by 6.76% and undershoot of one-via hole changes by 7.83%. Overshoot of three-via hole changes by 8.75% and undershoot 9.74%. The reflection portion of signal increases with the via hole number. As for high-speed PCB, these changes are relatively big to the circuit performance.

The parasitic inductance and capacitance increase with the via hole number. And so is the signal reflection. The increase of the via hole number not only increases the time delay, but also the signal reflection. From the point of waveform, wave quality becomes bad when the via hole number increases.



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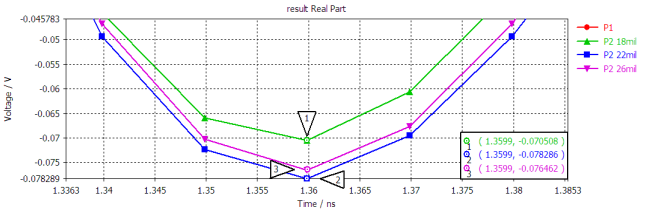
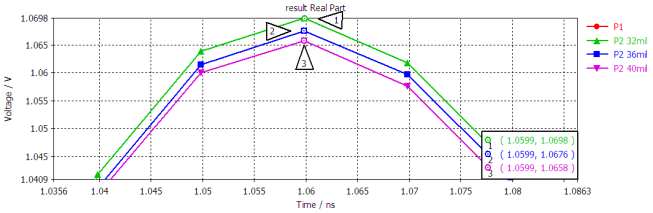


(b)

Fig. 8. Different pad diameters (a)overshoot (b)undershoot



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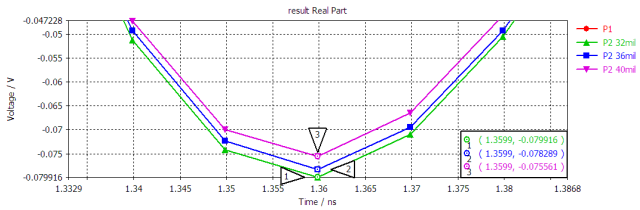

(b)

Fig. 9. Different aperture diameter (a)overshoot (b)undershoot

As shown in Fig. 8 and 9, the transmission line with a via hole changes the maximum of the 8 percent. When the via diameter changes 8mil, the overshoot changes 1.6% and the undershoot 0.8%. When the aperture diameter changes 8mil, the maximum changes 0.4%. Therefore, the reflection portion of the signal increases with the pad diameter and decreases with the aperture diameter. In addition, the effect of the via diameter on the maximum is greater than that of the aperture diameter.

V. CONCLUSION

In high-speed PCB, a proper design in via holes will save costs, decrease electromagnetic interference and reduce radiation. However, the effect of parasitic parameters of the via hole shouldn't be ignored. This paper discusses transmission characteristics of via holes in time-domain. Results reflect time delay and signal reflection directly. Hence, through appropriate design in via holes, the validity and reliability in high-speed PCB will be increased.

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