Evolution of RF-IC with PLL synthesizer used in mobile terminals

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Abstract
This paper describes “the evolution” of RF-IC with PLL synthesizers used in mobile terminals. At first, a limitation of PLL is demonstrated for clarification of motivation to employ the fractional PLL. Secondly, driving force of the evolution of PLL is demonstrated with system requirements and technical roadmap for the chipsets and PLL synthesizers. Finally, SiGe RF-ICs for PDC and W-CDMA with PLL functionalities are demonstrated in this paper.

Key word
Phase locked loops, Radio communications, Mixed analog-digital integrated circuits

I. Introduction
Miniaturization and reduction of parts count are very important issues for mobile terminals. Research and development activities on RF-ICs have been conducted intensively. Most of circuit blocks are integrated toward SoC (System on Chip). In the following descriptions, “the evolution of the PLL synthesizer” is focused. Since 1960s, PLL has been used in frequency synthesis [1]. PLL components like a frequency divider and a phase detector have been integrated as “PLL-IC” on one chip since 1970s. Year by year, the shrinking lithography rule of the semiconductor is making PLL-IC die size smaller. Because of the improved circuit density, transceiver circuit blocks can be integrated with the PLL on the same die [2]. In this paper, overview of the evolution of the PLL synthesizer is described from the viewpoint of the transceiver system design.

II. System advantage of the fractional-PLL
In this section, switching-speed and phase noise of the PLL synthesizer are described to clarify the advantages of the fractional PLL [3]. The advantages motivate employment of the fractional-PLL synthesizer, although the fractional-PLL has penalties of higher current consumption and larger die size.

A. Switching speed with a delay component
Delay effect in frequency divider [4] is focused for the switching speed limitation. Figure1 shows a block diagram of the second order PLL synthesizer with the charge pump. \( f_{\text{ref}} \) is the reference frequency of the PLL, \( f_{\text{stp}} = f_{\text{ref}} / M \) is the channel step, and \( M \) is the modulo number of the fractional counter. With assumption of frequency step \( \Delta f \), transient behaviors of output frequency \( f_e(t) \) are given as follows:

\[
f_e(t) = L^{-1}[(1/2\pi) \cdot s \cdot \Theta_e(s)]
\]

\[
\Theta_e(s) = \frac{2\pi \cdot \Delta f}{s^2 + (2\zeta \cdot \omega_n \cdot s + \omega_n^2) \cdot \exp(-s/f_{\text{ref}})}
\]

where \( s \) is Laplace transform variable, \( L^{-1}[^{*}] \) is the inversion of Laplace transform, \( \omega_n = 2\pi \cdot f_n \) is the angular natural frequency, and \( \zeta \) is the damping factor. Transfer function of each component is described in Figure 1. In (1), the delay component of the frequency divider is expressed as \( \exp(-s/f_{\text{ref}}) \). Figure2 shows general representation of the transient behavior on the second order PLL with the delay component. This figure is calculated by “the FILT method” [5]. Horizontal axis of Figure2 is normalized by \( n \omega \). Higher \( n \omega \) enables higher speed under the limitation given by \( f_{\text{ref}} \). With higher \( f_{\text{ref}} \) of the fractional-PLL, the delay can be reduced and limitation of the switching speed can be improved, as shown in Figure3.

B. Phase noise
Near-carrier phase noise of the PLL synthesizer [6] is represented as \( N^2 \cdot L_{\text{ref}}(s) = (f_{\text{out}} / f_{\text{ref}})^2 \cdot L_{\text{ref}}(s) \). \( L_{\text{ref}}(s) \) is the noise power summation of a frequency divider, a reference oscillator, a phase detector, and a loop filter. The fractional-PLL with higher \( f_{\text{ref}} \) can reduce near-carrier phase noise and relax phase noise budget for VCO.

III. Driving force of “the evolution of PLL”
A. System requirement
To improve the system capacity in mobile TDMA systems like GSM and PDC, required switching speed becomes very high compared with analog systems. Moreover, low phase noise at adjacent channel is important for reducing interference between channels. For PLL synthesizers, switching speed and phase noise are in trade-off. This made the development of the fractional-PLL synthesizer for mobile TDMA systems a changeable item. In the third generation system like W-CDMA, required specification of the PLL synthesizer can be relaxed, because of wider/static frequency allocation. Multi-mode operations require high-speed
system hand-over like “compressed mode operation”. Thus, the required switching speed of the receiver is almost the same as for TDMA systems. Also, reduction of near-carrier phase noise is important to achieve good vector accuracy in multi-level modulation system like HSDPA. Thus, continuous improvement in speed and phase noise has been required from the first generation till future radio systems.

B. Chip sets roadmap for mobile terminals

To reduce parts count and materials cost, radio functionalities have been integrated rapidly toward SoC. In addition, more complex PLL architectures such as the fractional-PLL are required for performance improvement. Figure 4 indicates the technical roadmap of the chipsets used in mobile terminals. Based on Moore’s Law, the evolution of chipsets is in progress. In the past, there were following milestones for PLL developments:

- Employment of the fractional-PLL to reduce total PLL number in 2G terminals, as described in the PDC RF-IC (section IV).

Because of high RF performance on BJTs, BiCMOS process has been used for RF-IC’s in the past. With rapid progress of RF performances on CMOS, high gate/capacitor density of the standard CMOS process has motivated technical/business development toward SoC on the CMOS including RF, ABB and DDB. Thus, logic oriented circuit topologies are employed, step-by-step, as follows:

- The Σ–Δ modulation [8] like the MASH configuration for randomization of periodical spurious in fractional behavior, instead of analog means,
- The digitally controlled oscillator for higher integration including the loop filter and high yield of oscillation frequency [9].

C. Elementary techniques for the evolution

The PLL synthesizer has been evolving along with the improvements of the elementary techniques as follows:

1) Semiconductor techniques:
- High performance Transistor (SiGe, RF-CMOS)
- High-Q inductor (Multi-layer metal, Cu, Thick metal)
- High density capacitor (Multi-layer MIM) / gate
- Deep Trench Isolation

2) Circuit techniques:
- Integrated VCO with tank circuits [7]
- Σ–Δ modulator for Fractional-PLL [8]

3) Architecture techniques:
- Fractional PLL
- Logic oriented PLL with DCO [9]

Especially for fractional-PLL techniques, high-density process rule of less than quarter micron affords us the possibility to employ a more complex PLL like Σ–Δ modulator to reduce discrete spurious emission.

IV. SiGe RF-ICs for mobile terminals

A. SiGe PDC RF-IC

To achieve high speed and low phase noise with channel step of 25 kHz, the fractional-PLL configuration is employed for the synthesizer. Figure 5 shows a die photograph and a block diagram of the SiGe PDC RF-IC.
A transmitter without HPA, an IF receiver with an active-BPF, a fractional PLL and a multiplier are integrated on the 0.25μm SiGe chip with a die size of 3.35 mm x 3.35 mm. With the high-speed fractional-PLL synthesizer, one synthesizer configuration for both TX and RX can be achieved for the single duplex operation in PDC. This is very effective to minimize terminal size.

Table1 indicates evaluation results of the SiGe PDC RF-IC. The developed synthesizer can achieve low noise characteristic of -98 dBc/Hz@25kHz, and high-speed RF-IC. The developed synthesizer can achieve low noise characteristics can be achieved. Although measured phase noise and switching speed have no advantage over the PDC RF-IC, validation results are enough for the system.

V. CONCLUSION

The technical overview of RF-IC with PLL synthesizers used in mobile terminals is described. Furthermore, the PDC SiGe RF-IC and the W-CDMA SiGe TX-IC are demonstrated as design examples of PLL synthesizers.

ACKNOWLEDGMENT

The authors would like to thank Dr. Maher Abzaid, Mr. Alan Holden, Mr. Shigemi Hoshino and Mr. Ken Melvin of Texas Instrument for co-developing the PDC RF-IC; Dr. Dawn Wang, Duljit S. Malhi, Jack Kennedy and Norm Swanberg of IBM microelectronics previously for co-developing the W-CDMA TX-IC.

REFERENCES


Table 1 Summary of the Fractional- PLL synthesizer on the SiGe PDC RF-IC.

<table>
<thead>
<tr>
<th>RF Frequency</th>
<th>0.8 GHz band, 1.5GHz band</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference freq.</td>
<td>Variable, higher than 500 kHz</td>
</tr>
<tr>
<td>Channel step</td>
<td>25 kHz</td>
</tr>
<tr>
<td>Natural freq. *</td>
<td>7 kHz (0.8G)/4 kHz (1.5G)</td>
</tr>
<tr>
<td>Switching speed</td>
<td>less than 0.3 ms</td>
</tr>
<tr>
<td>Phase noise</td>
<td>-98dBc/Hz at 25 kHz</td>
</tr>
<tr>
<td>PLL current</td>
<td>2.9 mA without VCO</td>
</tr>
</tbody>
</table>

* Steady state after acquisition acceleration

Fig.5 A die photograph and a block diagram of the developed SiGe PDC RF-IC.

Table 2 Summary of the Integer-PLL synthesizer on the SiGe W-CDMA TX-IC.

<table>
<thead>
<tr>
<th>RF Frequency</th>
<th>2 GHz band</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference freq.</td>
<td>Variable, higher than 500 kHz</td>
</tr>
<tr>
<td>Channel step</td>
<td>200 kHz</td>
</tr>
<tr>
<td>Natural freq.</td>
<td>6 kHz</td>
</tr>
<tr>
<td>Switching speed</td>
<td>0.7 ms</td>
</tr>
<tr>
<td>Phase noise</td>
<td>-95dBc/Hz at 50 kHz</td>
</tr>
<tr>
<td>PLL current</td>
<td>14.7 mA with VCO</td>
</tr>
</tbody>
</table>

Fig.6 A die photograph and a block diagram of the developed SiGe W-CDMA TX-IC.