



Advance Program

3rd Pan-Pacific EMC Joint Meeting -PPEMC'08-



May 15-16, 2008
NTT Musashino R&D Center
Musashino, Tokyo, Japan

CHAIR'S MESSAGE

The Third Pan-Pacific EMC Joint Meeting 2008 (PPEMC'08) is held in Musashino, Tokyo after the last successful meetings in Okayama 2006 and in Hyogo 2005. The PPEMC is organized and sponsored as a second-kind international conference by IEICE (The Institute of Electronics, Information and Communication Engineers, Japan) Technical Group on Electromagnetic Compatibility (EMCJ). The objective of PPEMC meetings is to offer an opportunity to exchange information on the latest EMC topics to researchers in the Pan-Pacific region.



This time we have focused EMC problems concerning with printed circuit boards and transmission lines, which have become serious in designing modern instrument. Three active researchers in this field are invited to present their recent results, and thirteen regular papers are accepted from a viewpoint of conformity to the focused topics and the number limitation of presented paper. In IEICE Transactions on Communications issued in June, 2009, the Special Section after the Joint Meeting is planned. For the Special Section, we would like to solicit many paper submissions particularly from but not restricted to, researchers presenting their original works in the PPEMC'08.

Japan's International Symposium on EMC is held every five years and is rapidly growing bigger and more sophisticated. However, the period of five years is too long to keep EMC members in close contact with each other and to accommodate EMC novices. Thus the EMCJ committee launched the PPEMC to prepare for the coming international EMC symposium. The coming EMC symposium, EMC'09/Kyoto, will be held in Kyoto, on July 20 through 25, 2009. The next PPEMC will be held conjunctionally as a joint session in EMC'09. We also would like to invite many researchers/engineers in the Symposium.

I, as the chair of PPEMC'08/Musashino, Tokyo sincerely hope that this Joint Meeting could be significant to all the participants through a mutually beneficial information exchange, and person to person communications during the technical sessions, banquet, and so on. I also wish every participant has a pleasant stay in Musashino, one of the wonderful spots with natural environment in the season of fresh green in Tokyo, Japan.

Finally, I would like to express my sincere appreciation to the participating industries for their supports. I would also like to extend my heartfelt thanks to all the committee members of this meeting for their hard work in making the Joint Meeting meaningful.

A handwritten signature in black ink, consisting of the Japanese characters '上 芳夫' (Kami Yoshio).

Yoshio Kami
Chair of the Steering Committee of PPEMC'08

3rd Pan-Pacific EMC Joint Meeting PPEMC '08

**May 15-16, 2008
NTT Musashino R&D Center,**

3-9-11, Midori-cho, Musashino-shi, Tokyo, 180-8585, Japan

Organized and sponsored by:

The IEICE Technical Committee on Electromagnetic Compatibility (EMCJ)
and

The IEEE EMC Society Japan Chapter, Sendai Chapter

PPEMC '08 STEERING COMMITTEE

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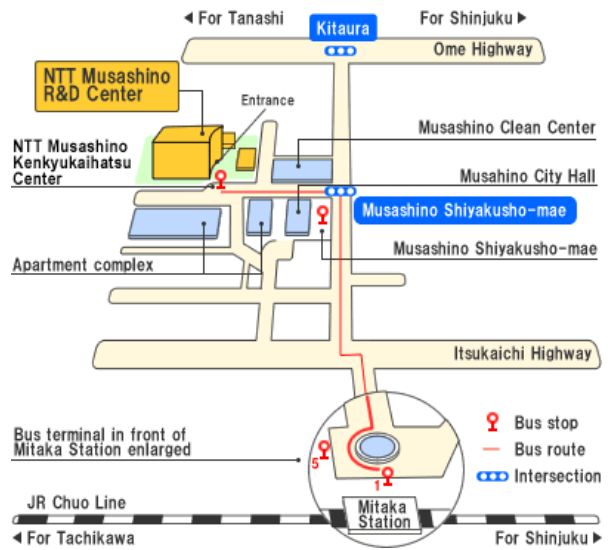
INFORMATION

Conference Site

Meeting Room, 2nd floor
Convention Hall A & B
NTT Musashino R&D Center
3-9-11 Midori-cho, Musashino-shi, Tokyo 180-8585
JAPAN
<http://www.ntt.co.jp/islab/e/access/index.html>
(Right figure)

Traffic

Attendees to PPEMC are recommended to take a taxi to the conference site. It requires 10 minutes and about ¥900-1,000 for a ride.
A bus is available from the north gate of JR Mitaka Station. Japanese language is necessary to utilize the bus service.



Registration

Registration desk will open in the conference site during the following hours.

May 15 (Thursday): 9:00 - 17:00

May 16 (Friday): 9:00 - 12:00

Registration fee (On-site): ¥8,000 (¥3,000 for a student)

Registration fee (Registration before 18 Apr. 2006): ¥7,000 (¥2,000 for a student)

Payment of the registration fee accepted at the on-site registration desk. This fee does not include the banquet.

Internet Service

The participants who have their own PC with IEEE 802.11a/b/g interface card can access free wireless LAN at the conference site.

Lunch

Lunch is available at "Restaurant Komorebi" located at the 1st floor of NTT Musashino R&D center.

Local Office

Mr. Kimihiro Tajima
NTT Energy & Environment Systems Labs. NTT Corp.
Tel.: +81-422-59-3482
Fax.: +81-422-59-3314
PPEMC@lab.ntt.co.jp

Exhibition

Time 10:00 to 17:00, May 15 to 16
Place Convention Hall
Exhibitor ROHDE&SCHWARZ Japan K.K.
Tektronix Japan, Ltd.
Yokogawa Electric Corporation

SOCIAL PROGRAM

Banquet

Time 17:30 to 19:30, May 15 (Thursday)
Place Club Kagei (a restaurant inside the NTT R&D center)
Fee ¥5,000 per person (¥3,000 for a student)

The people who will attend the banquet should make an appointment till May 9.
E-mail address: PPEMC@lab.ntt.co.jp

The banquet would be held in a simple and in informal style. All the participants are welcome to enjoy this buffet party. Any language is welcome there.

INSTRUCTIONS FOR ORAL SESSIONS

Working Language

The working language of the Symposium is English.

Visual Equipment

Conference room is provided with one PowerPoint projector for Windows and one PC for presentation with a CD-ROM or a USB memory. WINDOWS XP/Vista and Power Point are installed in the PC for presentation use. The speakers could either bring their own PCs for PowerPoint display, or copy their PowerPoint files to the PC in the conference room and confirm the file behavior before the session starts.

Session Registration

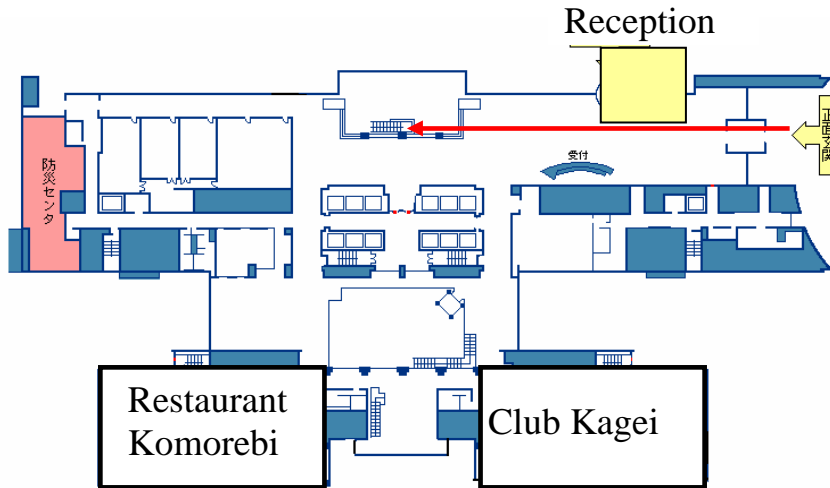
In order to ensure that the program runs smoothly, all speakers and session chairpersons are requested to contact the session desk at least 15 minutes before their sessions begin.

Presentation Time

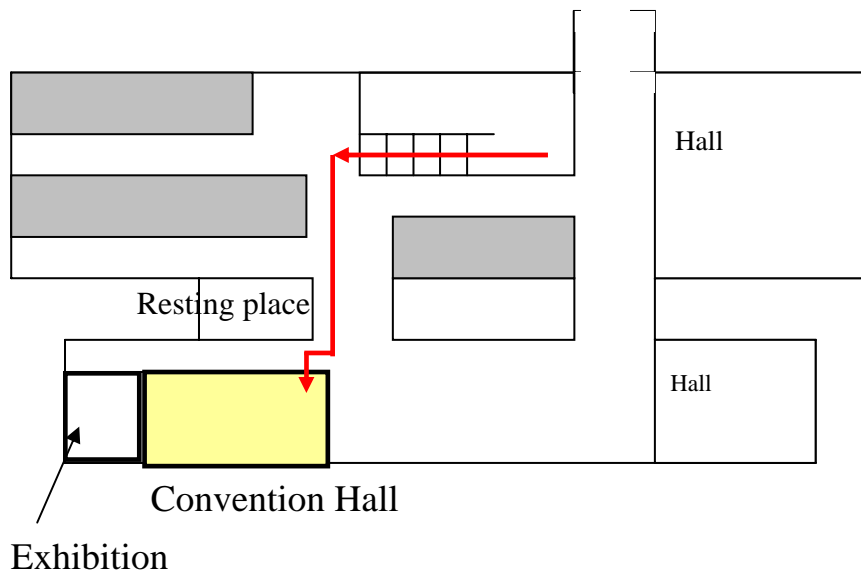
Each paper, except Invited Talks, has 20 minutes for presentation and 5 minutes for discussion.

GUIDE MAP

The First Floor



The Second Floor



TECHNICAL PROGRAM

Thursday, 15 May

Opening address

10:00 - 10:10

Yoshio Kami, *University of Electro-Communications, Japan*

Session 1 PCB and Circuit Design for EMC Control(1)

Time 10:10 to 11:50

Chair **Jun Fan**, *Missouri University of Science and Technology, USA* and **Naoto Oka**
Mitsubishi Electric Corp., Japan

15S1-1. Electromagnetic Characteristic of Printed Circuit Boards connected by Flexible Printed Circuit Board

Masayuki Ota, Takeshi Sakusabe, Takehiro Takahashi and Noboru Schibuya, *Takushoku University, Japan*

15S1-2. Time-domain Analysis of Two Parallel Traces on PCB

Fengchao Xiao¹, Mai Ikeda¹, Kimitoshi Murano² and Yoshio Kami¹,
¹*University of Electro-Communications*, ²*Tokai University, Japan*

15S1-3. Importance and Limitations of Modeling Parasitic Capacitance Between Package and PCB for Power Bus Noise and Radiation

Umberto Paoletti, Takashi Hisakado, and Osami Wada, *Kyoto University, Japan*

15S1-4. Common-Mode Radiation of Combined Boards Deduced from the Common-Mode Antenna Model

Makoto Torigoe^{1,2}, Akifumi Sadatoshi⁴, Tetsushi Watanabe³, Yoshitaka Toyota³, Kengo Iokibe³, Ryuji Koga³ and Osami Wada⁵, ¹*Okayama University*, ²*Hitachi, Ltd.*, ³*Okayama University*, ⁴*Industrial Technology Center of Okayama Prefecture*, ⁵*Kyoto University, Japan*

Session 2 PCB and Circuit Design for EMC Control(2)

Time 13:15 to 14:30

Chair **Sungtek Kahng**, *University of Incheon, Korea* and **Osami Wada**, *Kyoto University, Japan*

15S2-1. An Experimental Investigation of Radiated EMI from a PCB-Chassis System: The case where the PCB is mounted vertically over the chassis plate

Naoki Kobayashi¹, Ken Morishita¹, Takashi Harada¹, Todd Hubing², Takahiro Yaguchi³, Akira Wakui³, Mitsuyoshi Kobayashi⁴, Akinobu Kawata⁴ and Hidenori Muramatsu⁵,
¹*NEC System Jisso Research Laboratories, Japan*, ²*Clemson University, USA*, ³*NEC Informatec Systems*, ⁴*NEC Engineering*, ⁵*NEC Access Technica, Japan*

15S2-2. A Study on Effect of Noise Suppression Sheet on EM Radiation from a PCB

Yoshiki Kayano and Hiroshi Inoue, *Akita University, Japan*

15S2-3. Study on Noise Reduction Effect Using the Decoupling Capacitor with Resistor on Power Distribution Line
Takeshi Hakoda, Takashi Sakusabe, Takehiro Takahasi, and Noboru Schibuya, Takushoku University, Japan

Banquet

17:30 - 19:30 , May 15 (Thursday)

Club Kagei (a restaurant inside the NTT R&D center)

Friday, 16 May

Session 3 Invited Session

Time 9:30 to 12:10

Session 3-1

Invited Session (1)

Time

9:30 to 10:20

Chair

Yoshio Kami, University of Electro-Communications, Japan

16S3-1. Methodology to Tackle the Noise Against the Signal Integrity for Slit PCB Power/Ground Planes (Invited)
Sungtek Kahng, University of Incheon, Korea

Session 3-2

Invited Session (2)

Time

10:25 to 11:15

Chair

Hiroshi Inoue, Akita University, Japan

16S3-2. High-speed Channel Loss in PCB and Equalizer Designs (Invited)
Joungho Kim, Korea Advanced Institute of Science and Technology, Korea

Session 3-3

Invited Session (3)

Time

11:20 to 12:10

Chair

Osamu Fujiwara, Nagoya Institute of Technology, Japan

16S3-3. Novel Electromagnetic Bandgap Structures for Parallel-Plate Noise Suppression in Printed Circuit Boards (Invited)
Tzong-Lin Wu, National Taiwan University, Republic of China

Session 4 **Coupling and Crosstalk**

Time 13:30 to 15:10

Chair **Jounggho Kim**, *Korea Advanced Institute of Science and Technology, Korea* and
Toshikazu Sekine, *Gifu University, Japan*

16S4-1. Independent Component Analysis-based Noise Monitoring System for Multiple EMI Problems

Masao Masugi, Ryuichi Kobayashi and Kimihiro Tajima, *NTT Corporation, Japan*

16S4-2. Balanced Bridge Circuit Concept for Suppressing Cross-Talk Noise between Two Perpendicular Signal Traces on Printed Circuit Boards

Tsuyoshi Maeno¹, Yukihiro Sakurai¹ and Osamu Fujiwara², ¹*DENSO Corporation*, ²*Nagoya Institute of Technology, Japan*

16S4-3. A Study of Cross-Talk between Microstrip-Lines on a Printed Circuit Board with Narrow Width

Yasuhiro Kudo, Teruo Tobana and Takayuki Sasamori, *Akita Prefectural University, Japan*

16S4-4. Crosstalk Analysis between Microstrip Lines Intersecting in Arbitrary Directions on Adjacent Layers in Multi-Layer PCB

Sang Wook Park, Shougo Matsuda, Fengchao Xiao and Yoshio Kami, *University of Electro-Communications, Japan*

Session 5 **Transmission Lines and Cables**

Time 15:40 to 16:30

Chair **Tzong-Lin Wu**, *National Taiwan University, Republic of China* and **Noboru Schibuya**,
Takushoku University, Japan

16S5-1. A Model of Signal Propagation along a Microstrip Line Crossing over a Slit in Ground Plane for Waveform Simulation

Makiko Ishida¹, Tohlu Matsushima¹, Yoshitaka Toyota¹, Tetsushi Watanabe², Kengo Iokibe¹ and Ryuji Koga¹, ¹*Okayama University*, ²*Industrial Technology Center of Okayama Prefecture, Japan*

16S5-2. Analysis of Nonuniform Transmission Line Equations using Yee-lattice and Wavelet Expansion

Kazunori Watanabe¹, Toshikazu Sekine¹, Yasuhiro Takahashi¹ and Kunikatsu Kobayashi², ¹*Gifu University*, ²*Yamagata University, Japan*

Closing address

16:30 - 16:40

Hiroshi Inoue, *Akita University, Japan*

Call For Papers

IEICE Transactions on Communications Special Section on 3rd Pan-Pacific EMC Joint Meeting -PPEMC'08- Topics of EMC on Transmission Line and Printed Circuit Board

The IEICE Transactions on Communications announces a forthcoming IEICE Special Section on 3rd Pan-Pacific EMC Joint Meeting –PPEMC'08- to be published in June 2009.

Growth of the high-speed and wide-band electronic system has accelerated to raise the Electromagnetic Compatibility (EMC) problems to the function of all of the electronic equipment. Most of the electronic systems use the signal transmission line on the printed circuit board. As it is believed that the source of the Electromagnetic Interference (EMI) is related to the signal transmission, the topic of the PPEMC'08 is on the EMC problems concerning with the signal transmission and the printed circuit board.

The objective of this Special Section is to discuss technical issues on EMC which provides next generation EMC design, EMC evaluation, EMC simulation and EMC mitigation techniques, and to discuss problems on the EMC test and measurement techniques, specifically focused on EMC technologies presented in the 3rd Pan-Pacific EMC Joint Meeting –PPEMC'08-. The Special Section solicits paper submission particularly from but not restricted to, researchers who presented their original works in the –PPEMC'08.

Scope:

The specified topic of the special section is focused on the EMC problems related to the transmission line, the printed circuit board (PCB). The other EMC issues related to PPEMC'08 would be acceptable.

All of the related EMC issues on the transmission line and the PCB

Submission Instructions:

Papers should be prepared according to the guideline given in the “Information for Authors” available at the web site http://www.ieice.org/eng/shiori/mokuji_cs.html, and must be submitted by **September 1st, 2008**. The length of the paper is recommended to be 8 printed pages. Prospective authors are requested to follow the submission process described below.

1. Submit papers using the IEICE Web site https://review.ieice.org/regist_e.aspx. E-mail submission and postal mail are NOT acceptable. Authors should choose the [Special-EB] 3rd Pan-Pacific EMC Joint Meeting –PPEMC'08- as a “Type of Issue/Category of Transactions” on the online screen. Do not choose [Regular-EB] Communications or other special sections.

2. “Copyright Transfer and Page charge Agreement” and “Confirmation Sheet of Manuscript Registration” must be sent by postal mail to the following address (secretariat of this issue) also before **September 1st, 2008**. Please mark “Special Sections on 3rd Pan-Pacific EMC Joint Meeting –PPEMC'08-” on the envelope.

Osamu Fujiwara
Nagoya Institute of Technology
Gokiso-cho, Syowa-ku, Nagoya, 466-8555 Japan
Tel: +81-52-735-5421 Fax: +81-52-735-7129 E-mail: fujiwara@odin.elcom.nitech.ac.jp

Special Section Editorial Committee:

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Yoshio Kami (University of Electro-Communication)

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*Please note that if accepted for publication, all authors, including authors of invited papers, should pay for the page charges

covering partial cost of publication. Authors will receive 50 copies of the reprint.

* At least one of the authors must be an IEICE member when the manuscript is submitted for review.

Invited papers are an exception.