A CMOS Square-Rooting Circuits

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Abstract

The article proposes the square-rooting circuit. It bases the square-law characteristics of CMOS operating in saturation region for generating square-root function. The principle of the research is attained by the current-mirror circuit, which controls the voltages. The designed circuit dominates current as input and voltage as output. The structure of the circuit is simplified by only seven CMOS. Simulation results are demonstrated by PSpice program. They find that an input range is about 3µA whereas ±1.5_V supply voltage.

1. Introduction

The signal compilation technology has been developed in great leap. The analog system offers many functional circuits such as multiplied circuit, positive, negative circuit, divided circuit, and squaring circuit. The square-rooting circuit as one of the useful analog circuit blocks, and another widely-used one is square-rooting circuit, which has also been proposed in various designs [1]-[3]. More research has built on the previous one [3] by depending on one single output, instead of the difference of two currents.

In this paper, we propose a new square-rooting circuit. The proposed circuit can be operating under the condition of saturation region and low power supply. The designed circuit using seven CMOSs gives the results that closely replicate the theory. It is functioning on voltage mode and current mode; current input and voltage output. The designed circuit is a compact and simplified version of this latest circuit-design technology.

2. Principle of Operation

The proposed circuit operates by having CMOSs work in the saturation region, based on the current-mirror circuit. The drain current equation is shown:

\[ I_D = K(V_{GS} - V_T)^2 \]  \hspace{1cm} (1)

Given that \[ K = \left( \frac{\mu_0 C_{OX}}{2} \right) \left( \frac{W}{L} \right) \]

The circuits in use are negative and positive current mirror. Since the two circuits operate on the same basic idea with opposing poles, this designed circuit is explained in a positive current mirror as shown in figure 1. The M1 and M2 are CMOS that operate in the saturation region. The calculation is shown in equation (2)-(5)

\[ I_{D1} = K_1 \left( \frac{W}{L} \right) (V_{GS1} - V_{T1})^2 \]  \hspace{1cm} (2)

\[ I_{D2} = K_2 \left( \frac{W}{L} \right) (V_{GS2} - V_{T2})^2 \]  \hspace{1cm} (3)

Given that \[ K = K_1 = K_2 = \frac{\mu_0 C_{OX}}{2} \] and the relationship of the second and third equations is explained in the fourth equation.
\[
\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_{2}}{(W/L)_{1}} \frac{(V_{GS2} - V_{T2})^{2}}{(V_{GS1} - V_{T1})^{2}}
\]

(4)

Figure one indicates that the voltage \(V_{GS1} = V_{GS2}\) and the threshold voltage \(V_{T1} = V_{T2}\) of the CMOS are identical, which alters the ratio of the current mirror to be

\[
\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_{2}}{(W/L)_{1}}
\]

(5)

The circuit in figure 2 illustrates the design in previous research [3]. The output circuit operates on the difference of the two inputs (Differential Square-Rooting), and also the different ratio of the current mirrors. The third circuit is the new design of the square-rooting circuit. The size of CMOS M5 is indicated as one fourth of M3. The relationship can be explained in equations (6)-(13).

\[
I_{IN} = K_{3}(V_{B} - V_{SS} - V_{T})^{3}
\]

(6)

\[
I_{IN} = K_{5}(V_{A} - V_{T})^{2}
\]

(7)

Given that;

\[
V_{A} = \sqrt{\frac{4I_{IN}}{K_{5}}} + V_{T}
\]

(8)

\[
V_{B} = \sqrt{\frac{I_{IN}}{K_{3}}} + (V_{SS} + V_{T})
\]

(9)

Therefore, considering figure 3, the current relationship of M6 and M7 is;

\[
I_{D6} = I_{D7}
\]

(10)

Given that,

\[
I_{D6} = K_{4}(V_{A} - V_{O} - V_{T})^{2}
\]

(11)

\[
I_{D7} = K_{7}(V_{B} - V_{SS} - V_{T})^{2}
\]

(12)

The values of \(V_{A}\) and \(V_{B}\) are taken from equation (8) and (9) into equation (11) and (12) respectively. Therefore, from equation (10), we arrive at the output relationship of the square-rooting circuit in equation (13), given that all K values of the CMOS are equal.

\[
V_{O} = \sqrt{\frac{I_{IN}}{K}}
\]

(13)

3. Simulation Results

The simulation results are derived from PSpice program with MOSIS CMOS 0.5μm LEVEL3 technology. The ratio \((W/L)\) for all transistor are 100μm/10μm, except for M5 is 25μm/10μm for obtaining the current mirror ratio equal to 1:0.25 shown in table1 and the model of MOS transistor shown in table2. And the simulation results are shown in figure 4-7. The graph in figure 4 illustrates the relationship between input current and output voltage. It is found that the input of the square-rooting circuit has operation region as wide as 3.3μA at ±1.5 \(V\). Figure 5 shows output signal when input current is triangle signal at 1kHz. Figure 6 shows frequency response around 975.89kHz. And figure 7 shows spectrum of square-rooting circuit.
4. Conclusion

In this article, the square-rooting circuit that requires low power supplies operates by using CMOS in Saturation Region (Square’s law). The new designed circuit possesses enhanced capacity that entails only 7 CMOS units. And the circuits have dynamic input range $3.3\mu A$. The circuit has current as input and voltage as output. The simulation result is almost identical to the theory.

**Table 1:** The W/L ratio of the proposed circuit

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M4</td>
<td>100/10</td>
</tr>
<tr>
<td>M6,M7</td>
<td>100/10</td>
</tr>
<tr>
<td>M5</td>
<td>25/10</td>
</tr>
</tbody>
</table>

**Table 2:** The model CMOS of MOSIS0.5μm LEVEL3

* MOSIS MODEL AT 0.5U
  MODEL NMOS1 NMOS LEVEL=3 PHI=0.700000
  TOX=9.60000E-09 XI=0.200000U TPG=1
  + VTO=0.6084 DELTA=1.070000 ED=4.203000E-08
  KP=1.77480E-04
  + LD=493.4 THETA=1.821000 RSH=1.66800E+01
  GAMMA=0.5382
  + NSUB=1.129000E+17 NFS=7.150000E+11
  VMAX=2.79000E+05 ETA=1.86900E-02
  + KAPPA=1.610000E-01 CGSO=4.092000E+04
  + CGBO=3.76500E+04 MJ=0.76700
  CJSW=2.00000E-11
  + MSW=0.710000 PB=0.990000

* MOSIS MODEL AT 0.5U
  MODEL PMOS1 PMOS LEVEL=3 PHI=0.700000
  TOX=9.60000E-09 XI=0.200000U TPG=1
  + VTO=0.9352 DELTA=1.238000E-02 LD=5.244000E-08
  KP=4.49270E-05
  + LD=124.9 THETA=5.749000E-02 RSH=1.166000E+00
  GAMMA=0.4551
  + NSUB=8.071000E+16 NFS=5.908000E+11
  VMAX=2.296000E+05 ETA=1.193000E-02
  + KAPPA=9.366000E-01 CGSO=2.126000E+04
  + CGBO=3.68900E-10 MJ=0.48300
  CJSW=2.510000E-10
  + MSW=0.212000 PB=0.930000

**Figure 4.** The relationship of the input current and the output voltage

**Figure 5.** The output and input signals of the square-rooting circuit

**Figure 6.** Frequency Response
Figure 7. Spectrum of square-rooting circuit

References