A new CMOS squaring Circuit using Voltage/Current Input

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ABSTRACT
This paper proposes a new CMOS squaring circuit using voltage/current input. It consists of a mixed signal circuit and a basic squarer. Its major advantages over the other square are: this design can take two inputs (voltage input, current input), its output can be the square of a voltage signal or the square of a current signal. Simulation results are carried by PSpice program. They find that the circuit can operate at ±2V power supplies, the voltage input range is ±0.6V , the current input range is ±0.6μA , the current output range is 55.0 µA and the -3 dB bandwidth is 31MHz.

1. INTRODUCTION

Recently, the low voltage analog current mode and voltage mode circuit design has been widely increasing. Especially, the dramatically grows up of the portable equipment demand that prefers the minimum number of the battery cells for the volume weight and long battery life. Therefore, the supply voltage, now come to be one major constant of new circuit design. The CMOS technology is one good choice for this requirement and is interesting for analog circuit designing in the past two decades. There are many advantages, such as, low cost technology, small size, easily scaled and high packing density, low power consumption, and capable to operate under low supply voltage while the performance still maintains. Therefore, the squaring circuit is a mathematical function widely used in communication system and measurements such as Frequency Doublers, Peak Amplitude Detector, and Analog Multiplier. Most squaring circuits rely on the squaring feature of CMOS [1-6]. Squaring circuit can be categorized into two groups according to its input; voltage squaring circuit [1-3] for voltage mode and current squaring circuit [4-5] for current mode. However, this article presents the circuit that operates in both voltage and current modes. The contemporary circuit combines the benefit of two different circuits. Therefore, it offers higher-end applications.

This paper proposed a new CMOS squaring circuit using voltage/current input. The circuit operates all MOS transistor are in saturation region. The simulated of the proposed circuit by PSpice program, is carried out MOSIS 0.5μm transistor model. This circuit is very suitable for low-voltage application and IC implementation.

2. PRINCIPLE OF OPERATION

The proposed circuit consists of mixed-signal circuit and basic squaring circuit as shown in figure 1.

Fig.1. Block diagram of the proposed circuit

2.1 Mixed-Signal Circuit

Given the design that CMOS ratio is W/L and operates in saturation region. The drain current equation is written as follows;

\[ I_D = (V_{GS} - V_T)^2; V_{GS} > V_T, V_{DS} > V_GS - V_T > 0 \]  

(1)

When \( V_X \) and \( I_X \) are the inputs of mixed-signal circuit in figure 2. The circuit’s output represented by \( V_{OX} \), which illustrates the relationship of input current and drain current of the CMOS, as shown in equation 2

\[ I_X = I_{D2} - I_{D1} \]  

(2)

Fig.2. Mixed-signal circuit
Pluck (1) in (2), we have
\[ I_X = K(V_{OX} - V_{SS} - V_T)^2 - K(V_X - V_{OX} - V_T)^2 \]  \hspace{1cm} (3)

Achieve \( V_{OX} \) at
\[ V_{OX} = \frac{I_X}{2K(V_X - V_{SS} - 2V_T)} + \frac{V_{SS} + V_X}{2} \]  \hspace{1cm} (4)

### 2.2 Basic Squaring Circuit

\( V_{OX} \) is gate voltage of M3, and \( V_O \) is drain voltage of M3. Moreover, M3 and M4 operate as signal reverser. The relationship of \( V_X \) and \( V_{OX} \) is written as;
\[ I_{D1} = I_{D4} \]  \hspace{1cm} (5)

Pluck (1) in (5), we have
\[ K(V_X - V_{OX} - V_T)^2 = K(V_{DD} - V_{OX} - V_T)^2 \]  \hspace{1cm} (6)

Achieve \( V_{OY} \) at
\[ V_{OX} = \frac{I_X}{2K(V_X - V_{SS} - 2V_T)} + \frac{V_{SS} - V_X}{2} \]  \hspace{1cm} (7)

The output current is;
\[ I_O = I_{D1} + I_{D3} \]  \hspace{1cm} (8)

When \( I_{D1} = I_{D4} \) \hspace{1cm} (9)

The drain current equation is written as
\[ I_O = K(V_X - V_{OX} - V_T)^2 + K(V_{OX} - V_T)^2 \]  \hspace{1cm} (10)

Put in the value of (4) and (7) in (10);

\[ I_O = K \left( \frac{V_X - I_X}{A} - V_T - \frac{V_{SS}}{2} \right)^2 + \left( - \frac{V_X}{A} + \frac{I_X}{A} - V_T - \frac{V_{SS}}{2} \right)^2 \]  \hspace{1cm} (11)

When \( A = 2K(V_X - V_{SS} - 2V_T) \)

### 2.3 Complete Squaring Circuit

The circuit in figure 4 consists of two circuits from figure 2 and figure 3. The relationship between the input and the output can be written in the same way as in equation (12)
\[ I_O = K \left[ \left( \frac{V_X - I_X}{A} - \frac{V_{SS}}{2} + V_T \right)^2 \right. \]
\[ + \left( - \frac{V_X}{A} + \frac{I_X}{A} - \frac{V_{SS}}{2} + V_T \right)^2 \]  \hspace{1cm} (12)

When \( \frac{V_{SS}}{2} = -V_T \)

From equation 12, If \( I_X = 0 \) (no \( I_X \) input), the circuit operates as voltage-signal squaring circuit. Equation 12 can be written as;
\[ I_O = \frac{KV_X^2}{2} \]  \hspace{1cm} (13)

\[ I_O = \frac{I_X^2}{2K(V_X - V_{SS} - 2V_T)^2} \]  \hspace{1cm} (14)
Equations (13)-(14) demonstrate that the proposed circuit is compatible for both current and voltage inputs as selected.

3. OPERATION INPUT RANGE

The input range is calculated from the operational conditions of CMOS (M4 and M5) in saturation region; \( V_{GS} > V_T \) and \( V_{DS} > V_{GS} - V_T \).

Saturation condition of M4; \( 0 - V_{O2} > V_T \) \hspace{1cm} (18)

Using equation (9);

\[
\frac{I_i}{2K(V_i - V_{SS} - 2V_T)} + \frac{V_i}{2} > V_T + \frac{V_{SS}}{2} \hspace{1cm} (19)
\]

Saturation condition of M5; \( V_{O2} - V_{SS} > V_T \) \hspace{1cm} (20)

Using equation (9);

\[
\frac{-I_i}{2K(V_i - V_{SS} - 2V_T)} - \frac{V_i}{2} > V_T + \frac{V_{SS}}{2} \hspace{1cm} (21)
\]

From equation (19) and (21); the input range is written as;

\[
-V_T - \frac{V_{SS}}{2} > \frac{-I_i}{2K(V_i - V_{SS} - 2V_T)} - \frac{V_i}{2} > V_T + \frac{V_{SS}}{2} \hspace{1cm} (22)
\]

According to equation (22), the input range depends on \( V_{SS} \) and \( V_T \). Given that \( I_i = 0 \), \( V_{SS} = -2V \), \( V_T = 0.7V \), the input range is \(-0.6 > V_i > 0.6\). The operation input is widening by the increased power supply or selective CMOS with low \( V_T \).

4. SIMULATION RESULTS

The proposed squaring circuit has been simulated by PSpice program, using the model parameter of \( 0.5 \mu m \).

Level 3 CMOS process \( V_{TN} = 0.67V \), \( V_{TP} = 0.93V \) and the W/L ratio of CMOS is written in table 1.

Table1. The W/L ratio of the proposed circuit

<table>
<thead>
<tr>
<th>CMOS</th>
<th>W/L</th>
<th>( \mu m / \mu m ).</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M2</td>
<td>1/4</td>
<td></td>
</tr>
<tr>
<td>M3-M4</td>
<td>10/2</td>
<td></td>
</tr>
</tbody>
</table>

Figure 5A illustrates the simulation of voltage-signal squaring circuit. And figure 5B illustrates the simulation of current-signal squaring circuit. The simulation results are demonstrated as follows: The DC characteristic; (6A)-- \( V_i \) varies from \(-600mV\) to \(+600mV\) and (6B)-- \( I_i \) varies from \(-6\mu A\) to \(+6\mu A\), shows a wider input range of power supplies. The AC characteristic; (7A)-- \( V_i = 500mV \sin(200k\pi t) \) and (7B)-- \( I_i = 500mA(200k\pi t) \), gives the output signal as double frequency. The frequency response, (8A)-- \( V_i = 500mV \sin \omega t \) and (8B)-- \( I_i = 500mA \sin \omega t \), yields the cut off frequency around 31MHz. The simulation results are shown in figure 6-8.
The frequency response can be improved by decreasing the W/L ratio of the CMOS. However, doing so would significantly undermine the circuit’s accuracy.

5. CONCLUSION
The new squaring circuit consists of four CMOSs. The proposed circuit is compatible for both current and voltage inputs. The simulation results carried out by PSpice program specifies the operation voltage input range at ±600mV and the operation current input range at ±6μA. The circuit’s frequency response is approximately 31MHz at ±2V power supply.

6. REFERENCES