Analysis of Radiated Emission Performance of Various Passive Signal Integrity Improvement Techniques

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Abstract—The impact of passive signal integrity (SI) improvement techniques on the radiated emission (RE) for different interconnections between digital devices is presented. In high speed digital integrated circuits, SI is no longer the only issue for desired functional performance. RE is also critical for the functional performance and for compliance with EMC standards. Hence, it is important to understand the impact of SI improvement techniques on the RE of digital circuits under realistic conditions. Four passive SI improvement techniques are considered here: series termination, parallel termination, Thévenin termination, and AC termination. Straight and L-shaped interconnections are investigated. Digital devices at the two ends of the interconnections are modeled by Input/Output Buffer Information Specification (IBIS) models. The RE evaluation results can help designers to select the appropriate SI improvement technique taking into account RE requirements.

Keywords—signal integrity (SI), radiated emission (RE), Input-Output Buffer Information Specification (IBIS) models

I. INTRODUCTION

With the increasing speed and density of digital integrated circuits, the radiated emission (RE) of digital circuits also increases, which makes the signal integrity (SI) no longer the only important issue for desired functional performance. In addition, EMC standards also put constraints on the RE for commercial devices. Hence, it is critical to know at the design stage the impact of SI improvement techniques on the RE of digital circuits, although it is often ignored in conventional design flows because of the separation of SI design and RE analysis.

Previously this issue was addressed by using an analytical method based on dipole antenna theory to predict the RE performance of the circuit with series or parallel termination improvement techniques [1], [2]. Here, we extend the investigation to other passive SI improvement techniques [3]. Different from [1], [2], which investigated the RE of a straight interconnection between a resistive source and a capacitive load, the interconnections investigated here include both straight and L-shaped interconnections, which are placed between two dynamic digital devices, i.e., a dynamic source and a dynamic load. The digital devices are modeled using the

Input-Output Buffer Information Specification (IBIS) models, which are widely accepted in the industry because of proprietary protection and fast simulation time [4]. By integrating with IBIS models, an existing RE evaluation method [5] can be extended to compute the RE of the interconnections between high speed digital devices directly, which can be easily adopted for SI designers. The investigation about the RE impact of different common used passive SI
II. SIGNAL INTEGRITY IMPROVEMENT TECHNIQUES

The schematic diagram for the PCB interconnections without any SI improvement technique is shown in Fig. 1(a). The impact of the following four passive SI improvement techniques on the RE is analyzed:
1. Series termination technique, shown in Fig. 1(b)
2. Parallel termination technique, shown in Fig. 1(c)
3. Thévenin termination technique, shown in Fig. 1(d)
4. AC termination technique, shown in Fig. 1(e)

The series termination technique adds a resistor \( R_1 \) in series with the load. The parallel combination of \( R_1 \) and \( R_2 \) equals to \( Z_0 \). The two resistors serve as pull up and pull down resistors respectively. Although it has power consumption in the steady state, it reduces driver burden by supplying additional current to the load. The AC termination technique is to add a resistor \( R_{ac} \) and a capacitor \( C_{ac} \) in parallel with the load. As in the parallel termination, the \( R_{ac} \) value is matched to \( Z_0 \) to eliminate reflections. \( C_{ac} \) is used to reduce the steady state power consumption.

III. METHOD FOR RADIATED EMISSION PREDICTION

The RE prediction method used here is based on the method given in [5], [7]. The method computes the RE from the distributed current along the interconnection with the use of dyadic Green’s function. Note that an infinite ground plane and lossless microstrip line elements are assumed in this method.

A. Distributed Current along the Interconnections

The distributed current along the interconnections can be derived from the two-port voltages and currents extracted from circuit simulations with a commercial circuit simulator. The schematic diagram for the circuit simulation is shown in Fig. 1, in which both the driver and receiver are modeled with corresponding IBIS models. Fig. 2 represents the geometries of the two investigated interconnections: a straight interconnection and an L-shaped interconnection. In circuit simulations, the straight and L-shaped interconnections can be represented by equivalent two-port networks as shown in Fig. 3(a) and Fig. 3(b), respectively. The capacitance \( C \) in Fig. 3(b) models the bend corner of the L-shaped interconnection for simplicity [5]. The value of \( C \) can be calculated by the formula

\[
\begin{align*}
I_x (x) &= \frac{1}{2} \sin(\beta \sqrt{Z_0} x) (I_{in} e^{j\beta x} + I_{out} e^{-j\beta x}) - \frac{1}{2} \cos(\beta \sqrt{Z_0} x) (I_{in} e^{j\beta x} + I_{out} e^{-j\beta x}) \\
&\quad - I_{in} e^{j\beta x} - I_{out} e^{-j\beta x} + j \cos(\beta \sqrt{Z_0} x) \frac{V_{in}}{Z_0} e^{j\beta x} (1)
\end{align*}
\]

where \( l = x_s - x_e \). A similar expression is also obtained for the distributed current \( I_y(x) \) for the straight interconnection by replacing \( (V_{in}, I_{in}, V_{out}, I_{out}, l) \) with \( (V_{in}, I_{in}, V_{2}, I_{2}, I_{1}) \) or \( (V_{in}, I_{in}, V_{out}, I_{out}, l) \).

B. Far Field Dyadic Green’s Function

The RE can be directly computed from the distributed current with the dyadic Green’s function. The RE contributed by the \( x \)-directed current \( I_x(x) \) is defined as \( \overrightarrow{E}_x(\vec{r}) \), while the RE contributed by the \( y \)-directed current \( I_y(y) \) is defined as \( \overrightarrow{E}_y(\vec{r}) \). The calculation for \( \overrightarrow{E}_x(\vec{r}) \) and \( \overrightarrow{E}_y(\vec{r}) \) can be expressed as [5]

\[
\begin{align*}
\overrightarrow{E}_x(\vec{r}) &= \int I_x(x') G_x(x', \vec{r}) e^{j\beta x' \vec{r} \cdot \hat{\omega}} dx' \\
\overrightarrow{E}_y(\vec{r}) &= \int I_y(y') G_y(y', \vec{r}) e^{j\beta y' \vec{r} \cdot \hat{\omega}} dy'
\end{align*}
\]

where

\[
\begin{align*}
\vec{r} \cdot \hat{\omega} &= \vec{r} \cdot \sin \theta \cos \phi + y' \sin \theta \sin \phi + z' \cos \theta \\
G_x &= \frac{jq \mu_0}{4\pi} e^{-j\beta r} (\hat{\omega} \cdot \hat{x}) A_x(\theta, \phi)
\end{align*}
\]
C. Validate the Evaluation Method

In order to validate the method, RE comparison of the result by the proposed method and the result of the 3D full-wave simulator, ANSYS HFSS at r=3 m, \( \theta = \phi = 0^\circ \) for an L-shaped interconnection is shown in Fig. 4. The interconnection with \( W=4.9 \text{ mm} \), \( L_1=L_2=75 \text{ mm} \), \( \varepsilon_r=2.2 \) and \( h=1.6 \text{ mm} \) is between a 1 V voltage source with 50 ohm source impedance and a capacitive load with \( C=50 \text{ pF} \). It is observed that the RE result from this model agrees well with the RE result obtained from full-wave simulation.

IV. RADIATED EMISSION PERFORMANCE OF SIGNAL INTEGRITY IMPROVEMENT TECHNIQUES

The RE of the straight and L-shaped interconnections between digital devices with different passive SI improvement techniques is investigated using the proposed method. The straight interconnection has \( L=150 \text{ mm} \) and \( W=4.9 \text{ mm} \) and the characteristic impedance is around 50 \( \Omega \). The L-shaped interconnection has the same width \( W \) and \( L_1=L_2=75 \text{ mm} \). The substrate parameters for both interconnections are \( \varepsilon_r=2.2 \), \( \tan\delta=0.001 \) and \( h=1.6 \text{ mm} \). Two SN74LVC125A buffers from Texas Instruments are used as the driver and the receiver respectively. The driver is stimulated by a pulse input of 8 MHz, 50% duty cycle, \( t_i=t_f=2 \text{ ns} \), \( V_{high}=5 \text{ V} \), \( V_{low}=0 \text{ V} \).

A. Radiated Emission for Straight Interconnection

The comparison of the maximum RE at \( r=3 \text{ m} \) for the original circuit and the improved SI circuits in case of the straight interconnection is shown in Fig. 5. It is noted that the maximum RE for this geometry is generally around the z-axis (\( \theta=0^\circ \)). From Fig. 5, it is found that only the series termination circuit always has lower RE than the original circuit. The other three SI improved circuits have higher RE than the original circuit from 0.03 to 0.2 GHz. They have much lower RE in the range of 0.2-0.5 GHz and 0.8-1 GHz.
Since the RE is directly related to the current in the interconnection, the comparison result for the current at the output of the straight interconnection ($I_{out}$) can be used to explain the RE performance. The comparison of the current in the original circuit and the current in the improved SI circuits in time domain is shown in Fig. 6. It is found that the parallel termination and the Thévenin termination circuits have lower current peaks than the original circuit. However, they have a significant DC current in the steady state while the original circuit has zero DC current. The AC termination circuit has zero DC current, but the current peak is very significant and even larger than the original circuit. Only the series termination circuit has a smaller current peak and has zero DC current at the same time. The currents along the straight interconnection show similar phenomena. The Fourier transformed time domain current at the same position is shown in Fig. 7. It is found that only the series termination circuit always has a smaller current than the original circuit current. The other three improved circuits have much larger currents than the original circuit for frequencies below 0.2 GHz and have smaller currents only for the ranges of 0.2-0.5 GHz and 0.8-1 GHz. The trends of the RE performance follow the trends of the current in Fig. 7.

B. Radiated Emission for L-shaped Interconnection

The comparison of the maximum RE at $r=3$ m of the original circuit and the improved SI circuits in case of the L-shaped interconnection is shown in Fig. 8. For this geometry, the maximum RE is still generally around the z-axis ($\theta=0^\circ$). From Fig. 8, it is found that although the RE envelope for the L-shaped interconnection is different from the RE envelope for the straight interconnection in the frequency above 0.7 GHz, the series termination circuit is still the only improved circuit which has smaller RE than the original circuit over the whole frequency range. Similarly, the other three SI improved circuits have more RE than the original circuit in the range of 0.03-0.2 GHz, although they have less RE in the ranges of 0.2-0.5 GHz and 0.8-1 GHz.

The current comparisons for the L-shaped interconnection in the time domain and frequency domain show the same phenomena as the straight interconnection in Fig. 6 and Fig. 7. And the trends for the RE performance still follow the trends of the current. The impact of these SI improvement techniques on RE for both interconnection structures are consistent with their impact on the distributed currents.

V. CONCLUSION

Since SI design and RE analysis are usually separated in conventional design flows, the impact of SI improvement techniques on the RE is usually ignored. This issue is addressed here by the impact analysis of four different passive SI improvement techniques on the RE performances of the straight and L-shaped interconnections. The series termination technique is recommended, because out of the four passive SI improvement techniques, only the series termination circuit always has lower RE compared to the circuit without any SI improvement technique. By observing the current on the interconnection in time domain, it is concluded that the main advantage of the series termination technique is that it has smaller current peaks as well as zero DC current.

However, the series termination technique is applicable only for the case where the output impedance of the driver is smaller than the characteristic impedance of the interconnection. The other three techniques can be applied for more general cases, but the RE increases. The method presented here can be easily adopted to evaluate the RE for the interconnections between dynamic digital devices when these SI improvements or even more complicated improvements are applied. Further investigation could focus on the RE of more complicated interconnections and for higher frequencies.

REFERENCES