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A Novel Δ A/D Converter by Using Nonlinear Imperfect Differentiating Circuit whithout the Comparator

Osamu Kakita† Mizuki Motoyoshi† Masayuki Yamauchi† Tsuyoshi Otake‡ Mamoru Tanaka†

†Department of Electrical and Electronics Engineering, Sophia University
7-1 Kioi-cho, Chiyoda-ku, Tokyo 102-8554, Japan
‡Department of Media-Network Science, Tamagawa University,
6-1-1, Tamagawagakuen, Machida, Tokyo, 194-8610, Japan
Email: kakita@ieee.org

Abstract—Although the Δ modulation ADC is proposed, which have not been addressed as the main research target, that is replaced to Σ Δ ADC for the reason of a prediction filter problem. The Σ Δ ADC is composed by simple analog circuit and complicated digital circuit. Considering circuit cost reduction and conversion time, we recall the Δ modulation technique. In this paper, a new Δ ADC is proposed, which is realized by the imperfect differentiating circuit. Moreover, the comparator is eliminated on the ADC.

1. Introduction

The sigma delta analog-to-digital converter (Σ Δ ADC) is popular for audio system and metrology devices such as low frequency domains. It has some advantages of simple structure, robustness of circuit sensitivity and noise, pulse density output and high resolution. Also, it is constructed by switched capacitor, switched current and switched operational amplifier (OP-amp). The Σ Δ ADC is equipped with differentiator and integrator which behave the function of low pass filter for signal and high pass filter for noise respectively. This fucntion is called noise shape filter, so the high resolution is obtained by Σ Δ ADC[1]. Furthermore, a noise shape filter is enhanced by high order integrator[1]. In addition, to get more high resolution, the over sampling technique can be applied to Σ Δ ADC. Although the signal is sampled by very high frequency against nyquist frequency, so the noise floor is flattened [1]. On the other hand, the conversion speed of Σ Δ ADC is very slow. The Σ Δ ADC becomes to be complex circuit increasingly, because of these enhancements.

First, the strategy of circuit cost reduction for the Σ Δ ADC is considered. We focus the Σ Δ modulator, which is derived from an delta (Δ) modulator for disabling a prediction filter problem. If we solve this problem, we can recall the Δ ADC[2]. It means to achieve a integrator elimination on the circuit.

The other approach of circuit cost reduction is an OP-amp. An OP-amp based integrator, an OP-amp based differentiator and an unity gain buffer (UGB) is well known good stability, but it must concern gain error and offset error. The non-OP-amp circuits exist with imperfect integrator and imperfect differentiator as contrasted with integrator amplifier and differentiating amplifier respectively. The imperfect circuits are composed by passive elements of resister and capacitor. If the signal does not have to amplify, the substitution of these imperfect circuits is one of an alternative. So we consider the realization of ADC that is composed by imperfect circuits.

In this paper, we propose imperfect differentiator ADC. Usually, the comparator is requisite circuit between analog circuit and digital circuit. We succeed comparator elimination by using our proposal of new Δ ADC. The proposed method is verified by the circuit simulations and the experimental results.

2. Proposing New Δ ADC

2.1. Conventional Δ ADC

The block diagrams of Σ Δ ADC and conventional Δ ADC are shown in Fig.1.(a) and Fig.1.(b) respectively.

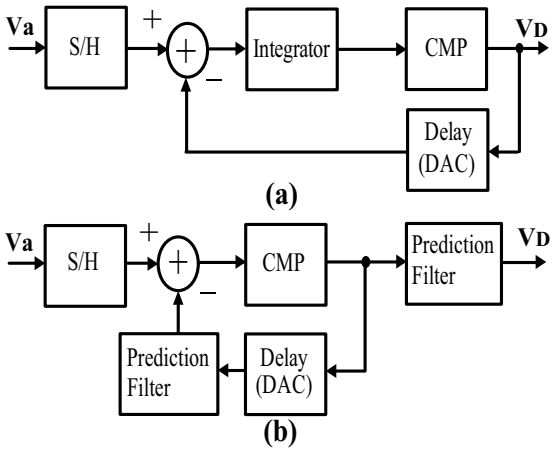

Figure 1: (a)Σ Δ ADC. (b)Conventional Δ ADC.

Usually, the prediction filter is composed by the integrator. The conventional Δ ADC compares with the Σ Δ ADC, an extra integrator is essential for proper operation. Furthermore, the Δ ADC has prediction filter problem potentially, which is caused by the phenomenon of whenever the magnitude of input signal changes drastically large.

2.2. Removing Prediction Filter

The ADCs of two types in Fig.1 are a single bit output, so the repetitive operations are required to obtain a quantization result. First, we exchange the single bit Δ ADC to multi bit Δ ADC. The efficiency of multi bit conversion is elimination of the iteration operations for quantization, which means no longer necessary the feedback loop between latter part of sample-and-hold (S/H) and digital circuit. Moreover, we consider to remove the prediction filter. If we attain the delta value between $n-th$ input and $(n-1)-th$ input, the prediction filter can be removed from Δ ADC. The multi bit Δ ADC is shown in Fig.2. The input voltage of $n-th$ input and $(n-1)-th$ is represented as $V_{a(n)}$ and $V_{a(n-1)}$ respectively. The input of odd number is held by S/H1, and the input of even number is held by the S/H2. The ideal quantized $n-th$ delta of $V_{D(n)}$ is given by

$$V_{D(n)} = V_{a(n)} - V_{a(n-1)}. \tag{1}$$

The configuration of Δ ADC in Fig.2 is equipped with two S/Hes. Secondly, for the circuit cost reduction, we consider the one S/H elimination. Although, the prediction filter does not exist in Fig.2 configuration, the quantization of delta between present input and previous input is usefulness. We propose always the input voltage is compared to the ground level. A S/H can be removed by this proposal. The block diagram of this proposal is shown in Fig.3. The ideal quantized $V_{D(n)}$ of $n-th$ input voltage is given by

$$V_{D(n)} = V_{a(n)}. \tag{2}$$

Also prediction filter does not exist on the Fig.3, so the proposed method of this configuration is a solution of prediction filter problem on the conventional Δ ADC.

2.3. Imperfect Differentiator

For the circuit cost reduction, we propose the OP-amps elimination on the Δ ADC. There are no prediction filter and feedback loop on Fig.3 configuration, so we do not have to concern the stability of feedback loop. Also, the output of differentiator does not need amplify. In such situation, we can implement the imperfect differentiator to the Δ ADC.
On the other hand, we focus the function of quantizer. The quantizer is the bridge between analog circuit and digital circuit, which send $'0'$ or $'1'$ to the digital circuit. Usually, a quantizer is composed by the comparator, which generates 2 values of low level and high level. Basically, the high level is recognized by the digital circuit when the voltage is more than threshold voltage, also the low level is recognized by the digital circuit when the voltage is less than threshold voltage. So the digital circuit has the comparator function potentially. We propose to use this function as the digital quantizer. The digital quantizer output q_k is defined by

$$q_k = \begin{cases} 1 & V_{delta} \geq V_{OH}, \\ 0 & V_{delta} < V_{OH}, \end{cases} \tag{3}$$

where the V_{delta} is output of imperfect differentiator and the V_{OH} is threshold voltage on digital circuit. The digital circuit recognizes high level as $'1'$ when the differentiation voltage greater than the threshold voltage. So OP-amp on a quantizer is eliminated from Fig.3 configuration by this implementation. The block diagram of proposed imperfect differentiator Δ ADC is shown in Fig.4, which is composed by S/H, imperfect differentiator, and digital circuit. Always the input signal V_a is compared to grand level, then the differentiation wave is generated by the differentiator, which is transferred to the digital circuit directly. The digital circuit receives the differentiation wave.

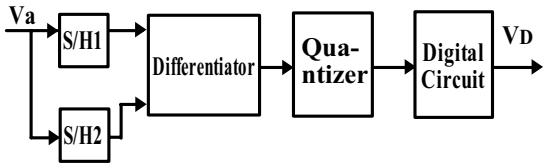

Figure 2: Multi bit Δ ADC.

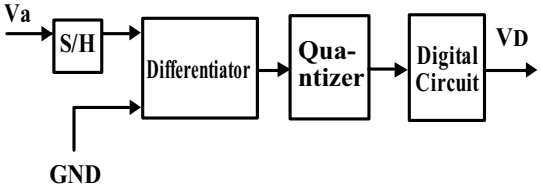

Figure 3: GND level Δ ADC.

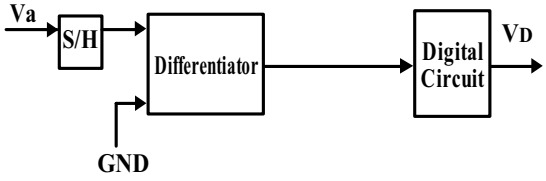

Figure 4: Imperfect differentiator Δ ADC.

Proposing method is convert input voltage to the time scale. The Δ ADC is counting the time during digital circuit is recognizing the high level. The output voltage of imperfect differentiator V_{delta} is given by

$$V_{delta} = V_a e^{-t/CR}, \tag{4}$$

where C and R is capacitor and resister respectively. So the gradient of this nonlinear curve can be controlled by the parameters of C and R. From equation (4), the equation (3) is represented as

$$q_k = 1 \quad when \;\; V_a e^{-t/CR} \geq V_{OH}, \tag{5}$$

the number of counter Q_k is given by

$$Q_k = nq_k, \tag{6}$$

where the n is number of counter. The configuration of Fig.3 can convert the negative voltage to digital value, but proposing Δ ADC is able to convert the voltage of more than threshold voltage, This weak point is recovered by the method of biasing input voltage more than threshold voltage in advance.

2.4. Discussion for Quantization

Actually, the counter value does not equal to quantized value, because of some error factors. The main factor is that the input of digital circuit is exponential curve. The other factors are mismatch of capacitance on analog circuit and error level zone on digital circuit. We propose to use the look-up table as the solution. The example of mapping table is shown in Fig.5. The counter value on digital circuit is mapped to digital value by this look-up talbe. The quantized value of V_D is decided by which the counter value compares to look up table. The counter is 5 bit, and V_D is 4 bit. If the counter registered between 11111 and 11100, the quantized value is 1111. Although, all inputs of digital circuit are nonlinear curve, so the quantization width on the counter does not uniform width. This method has the advantage of easy to calibration when the digital circuit is constructed by re-programmable device. The digital circuit cost of our proposal could be smaller than Σ Δ ADC which has decimation filter, digital filter, counter and divider.

2.5. Circuit Design

The analog ciruict on Δ ADC circuit is designed by switched capacitor (SC) technique. And the digital circuit is realized by the programmable logic device (PLD). The circuit of Δ ADC is depicted in Fig.6, which is composed by 1 OP-amp, 1 resistor, 1 CPLD, 2 capacitors and 6 analog switches. The S/H is composed by 1 OP-amp, 1 capacitor (C_{sh}) and 4 analog switches ($Sh1, Sh2, Sh3$ and $Sh4$). The Δ circuit is composed by 1 capacitor and 1 resistor. The $C1$ is

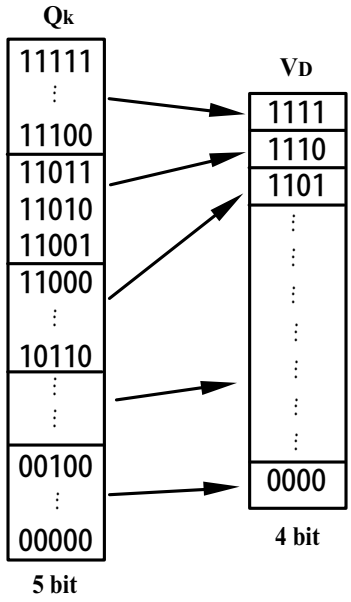

Figure 5: Look-up table for mapping.

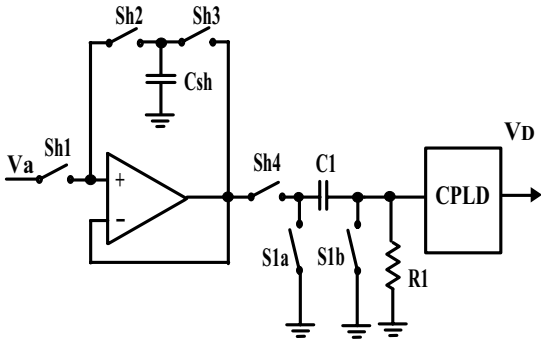

Figure 6: New Δ ADC Circuit.

charged off by 2 analog switches of S_{1a} and S_{1b}. This charge off operation contributes to comparing input signal to ground level.

3. Simulation Results and Experimental Results

3.1. Simulation Results

The designed circuit is confirmed by PSpice simulations. The input signal is AC $4.0V_{p-p}$ with 3.2V offset and 14MHz, S/H capacitor = 0.01μF, differentiator capacitor = 0.1μF, resister = 1KΩ and sampling rate is 100MHz. The simulation result and 2 phase clocks for switched capacitor circuit are shown in Fig.7. The counter is enabled 10 bit, then it compared to the 8 bit look-up table. This simulation achieved 8 bit resolutions. The efficiency of 2 analog switches of S_{1a} and

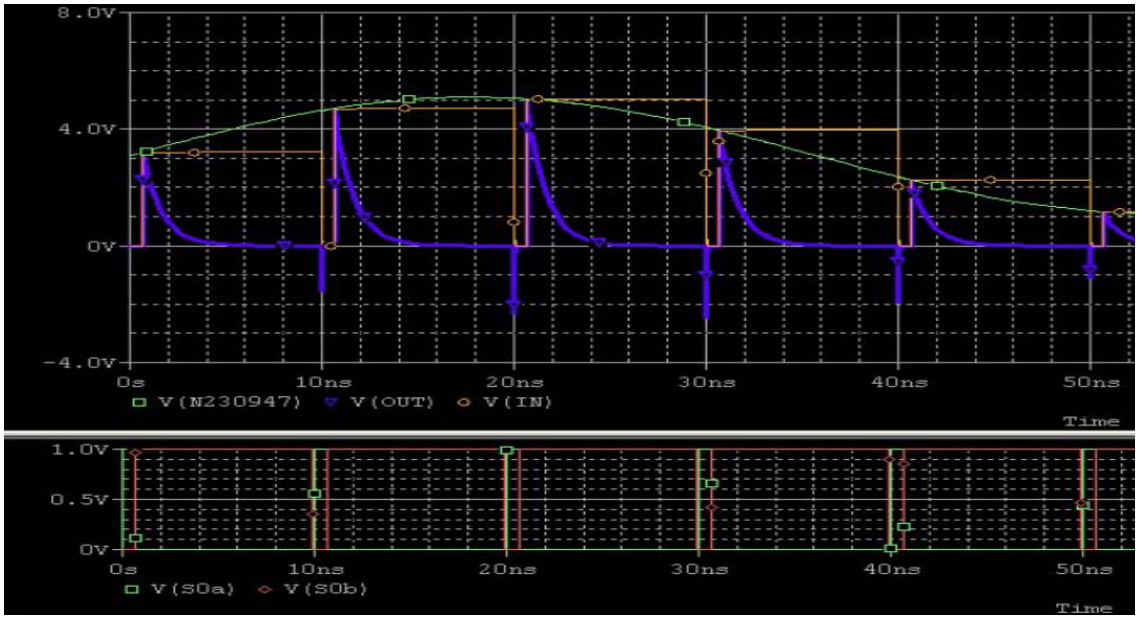

Figure 7: Simulation Results of new Δ ADC. Top: V(N230947) = input signal, V(OUT) = differentiator output, V(in) = S/H output. Bottom: 2 phase clocks for SC circuit.

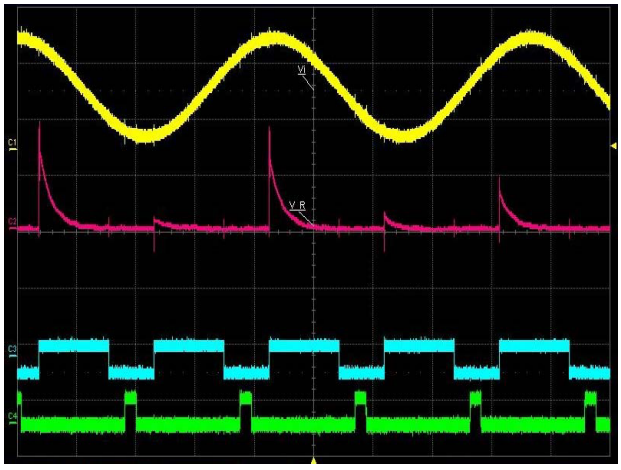

Figure 8: Experimental Results of new Δ ADC. C1: Input signal, C2: differentiator output, C3: clock 1 for SC, C4: clock 2 for SC.

S_{1b} is verified by this simulation.

3.2. Experimental Results

The Δ ADC circuit is realized by discrete ICs and CPLD. S/H and 2 analog switches are implemented by LF398F and DG419 respectively. The capacitor = 0.01μF, resister = 1KΩ. The XC95108 is used as CPLD. The input signal is AC 4.56KHz with 9.72V_{p-p}. The sampling frequency is 10.01KHz. One of the experimental result is shown in Fig.8. The DC 2.3V is biased to input signal. The CPLD could not have enough memory space for implementing look-up table, so the counter value is sent to PC via RS-232C port. The 135 times AD conversion achieved 6 bit resolutions when 8 bit counter is enabled.

4. Conclusion

In this paper, A new Δ ADC is realized, which is composed by imperfect differentiator. Our proposal succeeded circuit cost reduction, an OP-amp on the differentiator and a comparator are eliminated from conventional Δ ADC. Furthermore, the prediction filter problem of Δ ADC is solved by our proposal. Our proposal is verified by both simulation results and experimental results. The future work is to establish theoretical definition of creating look-up table for each resolution.

References

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[2] James C. Candy, "A Use of Double Integration in Sigma Delta Modulation," IEEE Trans. Commun., vol. COM-33, pp. 249-258, Mar. 1985.