

## A chaos-driven PLL based spread spectrum clock generator

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**Abstract**— Chaos-based frequency modulation has been shown to significantly reduce electromagnetic interference due to high frequency clock signals with respect to other methods. In this paper we present the design of a clock generator capable of generating a spread spectrum clock via chaotic frequency modulation. The proposed circuit is based on a conventional PLL whose VCO block is adjusted to allow simple and efficient frequency modulation.<sup>1</sup>

### 1. Introduction

Since growing operating speeds of today electrical devices may result in a high level of electromagnetic interferences, the problem of designing electromagnetic compatible (EMC) systems is of great practical concern. Several common solutions to increase system EMC, such as the adoption of power-supply filters, electromagnetic shields and filtered connectors, that aims at reducing the coupling between source and victim, suffer from several drawbacks; for example they can increase the overall cost, weight and dimension, or could not be employed at all, for example against intra-chip interferences. As the emitted energy is dangerous when it is very concentrated in spectrum [1], many methods have been presented to increment EMC of a system by spreading the delta-like power spectrum of periodic timing signals without compromising the proper operation of the circuit. This complies with the fact that Federal Communications Commission (FCC) regulations constrain peak power density spectrum of all signals in electronic equipments [2].

Many method have been proposed to alter a clock power spectrum; among them the so called spread-spectrum clock generation (SSCG) [1] which consists of a frequency modulation of the clock signal. Such technique was first proposed with the usage of periodic modulation laws, then improved in [3][4] with the introduction of random modulation, that allows to achieve a continuous spread of the interfering power thus reducing the spectrum peaks. Nevertheless, if the time between two frequency shifts in the output clock is large, i.e. the driving signal has low-frequency (slow modulation), EMC norm compliant signals may still cause failure in sensitive circuits, as a fixed frequency is maintained unaltered for a considerable period of time. The use of fast modulations [5] can prevent this.

In this paper we propose a SSCG based on a phase-locked loop (PLL). The PLL architecture is meant to externally set the center-spread frequency  $f_0$ , for example with an high-precision quartz oscillator. The proposed circuit performs a binary frequency modulation [6], that is a special case of frequency modulation when instantaneous frequency assumes only the two values  $f_0 - \Delta f$  and  $f_0 + \Delta f$ , each with probability  $p = 0.5$ , where  $\Delta f$  is the maximum allowed frequency deviation. The output frequency is set by a sequence of binary symbols  $\{x_k\}$  of length  $T = 1/f_M$ , typically coming from a random bit generator (RBG). Since performances of this modulation strongly depend on symbols uncorrelation, the use of a good RBG is recommended. We used a chaos-based generator as suggested in [7]; its block diagram, along with the implemented chaotic map, is shown in fig. 1. This architecture is very similar to that of pipeline analog-to-digital converters (ADCs) based on 1.5 bit/stage cells and it is proved to achieve very good results. In our implementation the pipeline is limited to two stages and there is no post-processing unit; this solution

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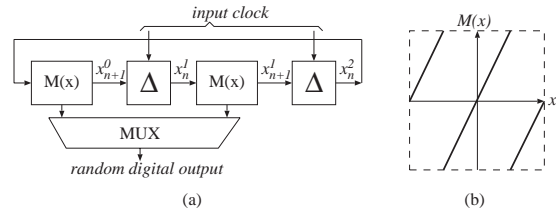


Figure 1: (a) Block diagram of the chaos-based RBG. (b) Implemented chaotic map.

ensures symbols uncorrelation high enough to achieve very good modulation performances. Also the lack of a post-processing unit, which is typically based on bits decimation, ensures a high working frequency; this is fundamental since our goal is to achieve a fast modulation, i.e. a very short time symbol  $T$ .

In binary modulation the only degree of freedom is the modulation index  $m = f_0/f_M$  which is used to flatten the power spectrum signal in the desired interval. A semi-analytical optimization [8] shows that the lowest peak on the fundamental tone is achieved by setting  $m \cong 0.318$ . The associated fundamental tone is quite flat and with a power level peak a few dB lower than the optimum slow modulation case. Such a  $m$  index is not optimum for flattening higher harmonics, that still feature peaks; yet, the power content of those harmonics is much lower than that of the fundamental and so are the corresponding peaks.

In the following we describe the PLL-based SSCG architecture in both spread-spectrum and non spread-spectrum mode. The system has been designed and simulated with a 3.3V 0.35 $\mu$ m CMOS double-poly triple-metal commercial technology. We also present results of circuit-level simulation of the SSCG working in spread-spectrum mode driven by the ADC-based chaotic map and compare them with the theoretical results, confirming the effectiveness of the proposed approach.

### 2. Circuit Description in non spread-spectrum mode

In non spread-spectrum mode the proposed circuit acts exactly as a conventional PLL-based clock generator. The block diagram is shown in fig. 2: it includes a reference clock oscillator, a Phase Frequency Detector (PFD), a Charge Pump (CP), a second-order

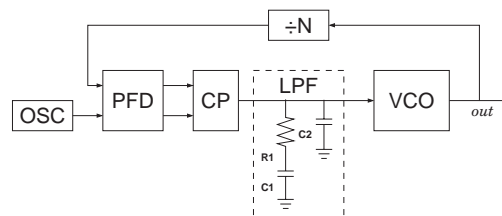


Figure 2: Voltage/Frequency characteristic of the VCO in non spread spectrum mode (solid line) and spread spectrum mode (dotted lines).

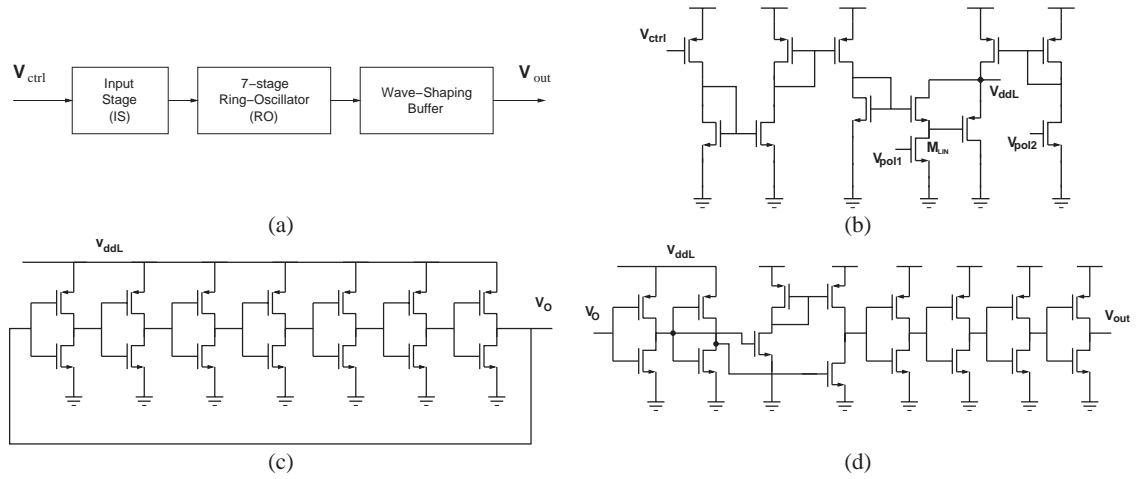


Figure 3: (a) Block diagram of the VCO. (b) Input Stage. (c) Ring-Oscillator. (d) Wave-shaping buffer.

Low-Pass Filter (LPF), a Voltage-Controlled Oscillator (VCO) and a divider by  $N$  on the feedback path.

#### Voltage-Controlled Oscillator

The proposed VCO is composed of an input stage (IS), a seven-stage ring oscillator (RO), and a wave-shaping buffer. Its diagram and schematics are shown in fig. 3 and are taken from [9].

The input stage of fig. 3-(b) supplies the correct operating current to the RO, as well as decouples it from the other parts of the circuit; the linearity of the IS is guaranteed by the transistor  $M_{LIN}$ , which works in the linear region acting as a negative feedback; the wave-shaping buffer shown in fig. 3-(d) is necessary to obtain proper values of logic levels and slew-rate in the output clock.

The solid line in fig. 4 shows the simulated voltage/frequency characteristic of the VCO, which is linear in a wide range of frequencies in the neighborhood of the central frequency  $f_0 = 100$  MHz. The VCO gain results equal to:

$$K_{VCO} = 82.5 \text{ MHz/V.} \quad (1)$$

#### Phase Frequency Detector

The most critical block in a PLL is typically the phase frequency detector (PFD). A low-precision PFD has a wide dead-zone (undetectable phase difference range), which results in increased jitter. The jitter caused by the large dead-zone can be reduced by increasing the precision of the phase frequency detector.

Fig. 5 shows the circuit diagram of the PFD, which is taken from [10]. Notice that conventional static logic circuitry is replaced by dynamic logic gates: as a result, the number of transistor in the PFD core is reduced to 16. The shortened feedback path delay and dynamic operation allow higher precision.

The PFD asserts both UP and DOWN outputs; if there is a phase difference between EXT\_CLK and VCO\_CLK, the width of UP and DOWN pulse will be proportional to the phase difference of the inputs.

#### Charge Pump and LPF

The schematic of the three-state charge pump is shown in fig. 6: its aim is to convert the UP and DOWN signals from the PFD into a current signal:

$$I_{out} = \begin{cases} I_{pump} & \text{UP} = 1 \\ 0 & \text{UP} = 0, \text{DOWN} = 0 \\ -I_{pump} & \text{DOWN} = 1 \end{cases} \quad (2)$$

Note that the value of  $I_{pump}$  is not explicitly indicated in fig. 6: it is set through  $I_{ref}$  and the ratio between the form factors of the current mirror branches;  $I_{out}$  is finally filtered by second-order LPF,

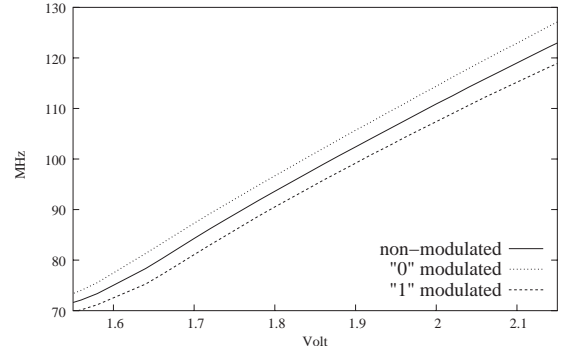


Figure 4: Voltage/Frequency characteristic of the VCO in non spread spectrum mode (solid line) and spread spectrum mode (dotted lines).

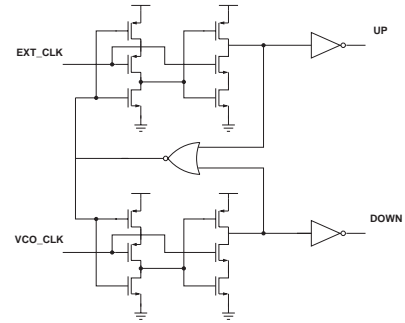


Figure 5: Phase Frequency Detector.

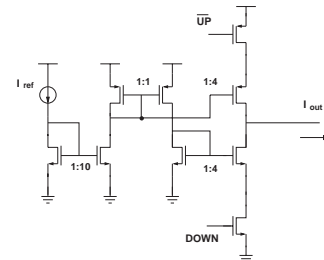


Figure 6: Charge Pump.

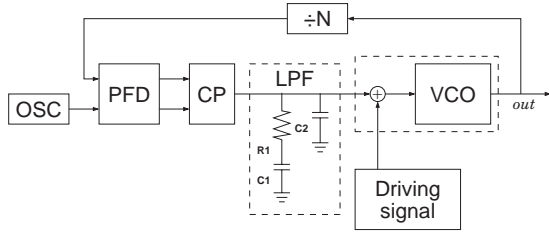


Figure 7: Block diagram of the PLL modified to achieve a frequency modulator.

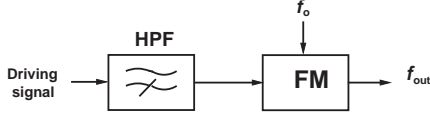


Figure 8: Equivalent model for a PLL-based frequency modulator.

which re-converts it into a voltage signal and generates the control voltage  $V_{ctrl}$  needed by VCO.

#### PLL model

The transient response of phase-locked loops is generally a nonlinear process that cannot be formulated easily. Nevertheless, as with other feedback systems, a linear approximation can be used to gain intuition and understand trade-offs in PLL design. Referring to the conventional linear model of the PLL in lock [11], the feedback system was studied and designed in order to ensure stability.

The resulting overall phase transfer function  $\phi_{out}(s)/\phi_{in}(s)$ , has a low-pass nature with a cut-off frequency:

$$\omega_n = \sqrt{\frac{I_{pump} K_{VCO}}{NC_1}}. \quad (3)$$

From (1) and (3), setting  $I_{pump} = 400\mu A$ ,  $N = 64$  and a cut-off frequency equal to 15 kHz, we have:

$$\begin{aligned} \omega_n &= 2\pi 15 \text{ krad/s} \\ C_1 &= 5.8 \text{ nF} \\ C_2 &= 58 \text{ pF} \\ R_1 &= 370 \Omega \end{aligned} \quad (4)$$

With these values, stability is guaranteed. Also, we can estimate the PLL lock-in time  $T_L$  as:

$$T_L = \frac{2\pi}{\omega_n} \approx 66\mu s \quad (5)$$

### 3. Circuit Description in spread-spectrum mode

In *spread spectrum* mode, the circuit is modified with the interposition of an analog adder between VCO input and LPF output (fig. 7). With this modification the PLL works as a frequency modulator. In fact, if we suppose that the driving signal is high frequency with respect to the PLL bandwidth  $\omega_n$ , we can notice that it drives the VCO as in an open-loop system, since it cannot pass through the feedback loop; furthermore, due to the negative feedback the low-frequency filter output sets the mean output frequency  $f_0$ , thus locking as in a conventional PLL-based clock generator. With these assumptions, the PLL can be considered as a frequency modulator, where the driving signal is the above input signal, and the carrier is the mean output frequency  $f_0$ . This of course works until PFD and VCO work in their linear region, i.e. when the frequency deviation  $\Delta f$  is not too large.

Actually, the equivalent model for this frequency modulation is the scheme shown in fig. 8, where the driving signal is filtered by

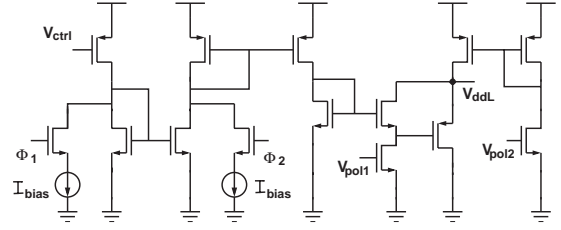


Figure 9: Modified VCO Input Stage.

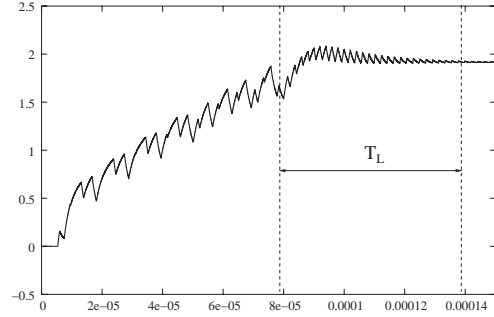


Figure 10: Simulation of the *pull-in* and *lock-in* process of the PLL.

a High-pass filter (HPF); from the linearized model of the PLL it can be shown that this HPF has a cut-off frequency equal to low-pass cut-off frequency  $\omega_n$  of the PLL in closed loop. Since our goal is to achieve a fast modulation, the bandwidth of the driving signal is very large with respect to the HPF cut-off frequency, and this scheme effectively works as a frequency modulator.

Due to the simple nature of binary modulation, very few changes are required in the non spread-spectrum mode circuit to implement this kind of modulation. Only the input stage of the VCO is modified as shown in fig. 9. The circuit is designed to work with  $\Phi_1 = \Phi_2 = \Phi$ , where  $\Phi$  is the signal coming from the chaotic map; however its behavior is more evident considering these two signals separately. Supposing  $\Phi_1 = \Phi_2 = 0$ , the circuit acts exactly as in non spread-spectrum mode. When  $\Phi_1 = 1$ , the current  $I_{bias}$  is subtracted from the current mirror, thus shifting up the  $V_{ctrl}/f_{out}$  characteristic. Otherwise,  $\Phi_2 = 1$  adds  $I_{bias}$  to the current mirror and shifts down the characteristic. The two modified characteristics, as well as the unaltered one, are shown in fig. 4; the difference between the curves, which is the PLL  $\Delta f$ , is set by the  $I_{bias}$  value. Modifying  $\Phi$  acts as shifting the output frequency between  $f_0 + \Delta f$  and  $f_0 - \Delta f$ , i.e. as binary modulating  $f_0$ . Experimentally, we have  $\Delta f = K_{\Delta f} I_{bias}$ , with:

$$K_{\Delta f} = 0.176 \text{ MHz}/\mu A \quad (6)$$

### 4. Experimental Results

The proposed SSCG has been designed and simulated in a  $0.35\mu m$  CMOS technology.

Fig. 10 shows the VCO control voltage during the pull-in process for the PLL in non spread-spectrum mode. We can notice that the PLL eventually reaches stability; also the time between entering the lock state (i.e. when major oscillations end) and reaching a complete settlement, is almost equal to the lock-in time  $T_L$  in (5).

Fig. 11 shows the power spectrum density of the output clock obtained from the circuit in spread-spectrum mode. In this simulation, the chaotic map frequency  $f_m$  is equal to  $f_m = 10$  MHz, so the frequency deviation is set to  $\Delta f = 3.18$  MHz to achieve the optimum frequency modulation index  $m = 0.318$  for the fundamental tone, i.e.:

$$I_{bias} = 18 \mu A \quad (7)$$

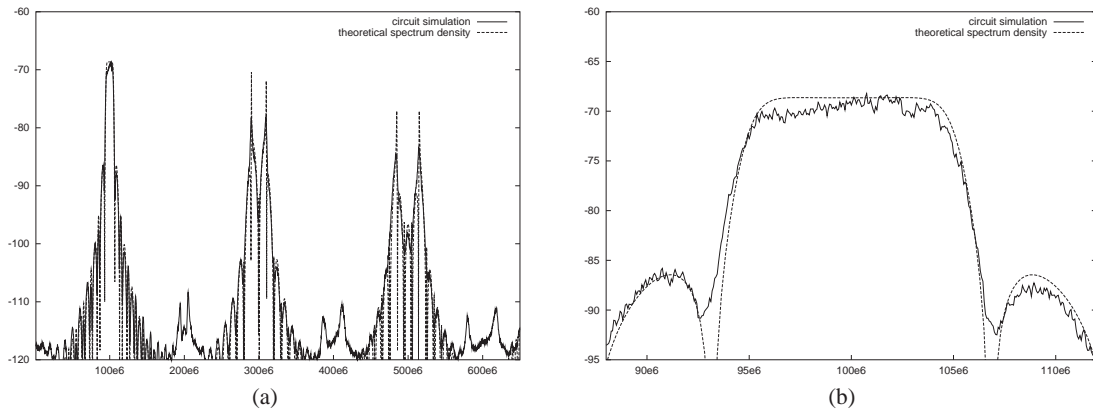


Figure 11: Comparison between power spectrum density of the output clock obtained from the simulated circuit and the theoretical power spectrum density of the binary modulation, for a wide set of harmonics (a) and only for the fundamental tone (b).

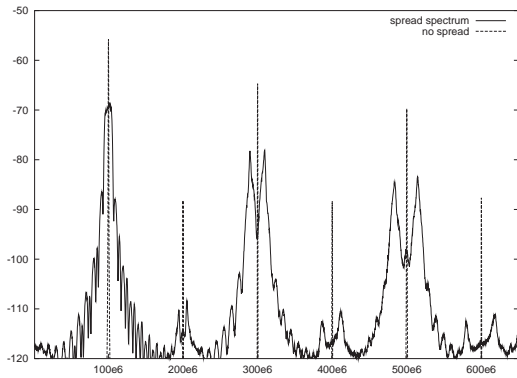


Figure 12: Comparison between power spectra density of the modulated and non modulated output clock.

This spectrum has been obtained by a 1.2 ms simulation and discarding the first 200  $\mu$ s data, which is a sufficient time, according to the bandwidth of the PLL, to consider all circuit transients extinguished. In this figure the expected theoretical power spectrum density from [6] is also shown. As can be seen, the simulated spectrum is very closed to the theoretical one.

Fig. 12 shows a comparison between the simulated power spectrum density of the output clock signal and the same spectrum obtained from the circuit without any driving signal, i.e. working as a standard PLL-based clock generator. The resolution bandwidth is set to 120 kHz, as indicated by CISPR regulations [2][12]. The comparison shows a peak reduction on the fundamental tone of about 13 dB.

## 5. Conclusion

In this brief, a SSCG is presented. This circuit can work both in non spread-spectrum mode and in spread spectrum mode, implementing a chaos-based binary frequency modulation. The circuit has been designed in a commercial CMOS technology and simulations have been shown; these simulations confirm that the proposed circuit works effectively as a binary frequency modulator, as expected from the circuit model. Furthermore, peak amplitudes of each harmonic are attenuated and the proposed architecture does achieve the spread-spectrum function as expected.

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