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Design Equations for Optimum Operation of Class E Amplifier with Nonlinear Shunt Capacitance at Any Duty Cycle

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Abstract– Design equations for satisfying optimum conditions of Class E amplifier with a nonlinear shunt capacitance with a grading coefficient of 0.5 at any duty cycle are derived. By exploiting sub-optimum class E operation, various amplifier parameters such as input voltage, operating frequency, output power, and load resistance can be set as design specifications. An example of a design procedure of the class E amplifier is given. The theoretical results were verified with Pspice simulation using SPICE MOSFET model Level 3.

1. Introduction

It is well known that the output capacitance of a MOSFET transistor is a nonlinear function of the drain-to-source voltage. The shunt capacitance of the class E amplifier consists of the nonlinear transistor output capacitance. Especially at very high operating frequencies, whole of the shunt capacitance consists of the transistor output capacitance. However, most analyses of class E amplifier have been done with linear capacitance.

An analysis of the class E amplifier with a nonlinear shunt capacitance of grading coefficient 0.5 was presented for the first time by Chudobiak for optimum operation at the duty cycle D = 0.5 [4]. This analysis was done only for the optimum operation at the duty cycle of D = 0.5. Authors have extended the Chudobiak analysis to sub-optimum operation and compared his results with linear shunt capacitance, subsequently. However, the analysis for the optimum operation at any duty cycle has not been done yet.

In this paper, design equations for the optimum operation at any duty cycle are derived for a class E amplifier with a nonlinear shunt capacitance of grading coefficient 0.5. In this analysis, expressions for all elements, peak switch voltage, peak switch currents, and output power capability are derived. A class E amplifier circuit was designed and its operation was verified with PSpice using Level 3 MOSFET model.

2. Voltage and Current Waveforms of the Class E Amplifier with Nonlinear Capacitance

The circuit analyzed in this paper is a class E amplifier shown in Fig. 1. The shunt capacitance of the amplifier consists only of the MOSFET output capacitance. The derivations of design equations are carried out under the following assumptions:

1) The inductance of the choke coil L_{RFC} is large enough to neglect its current ripple.
2) The internal resistance of the choke coil is zero; therefore, the DC voltage drop across the choke is zero.
3) The loaded quality factor Q of the output resonance circuit is high enough so that the output current can be considered a sine wave.
4) The load resistance includes parasitic resistances of the series resonance circuit, i.e., the resonance circuit is considered to be a pure reactance.
5) The MOSFET on-resistance transistor is zero.
6) The MOSFET turns on and off instantly.
7) The shunt capacitance C_1 is entirely comprised of the MOSFET output capacitance.
8) The grading coefficient of the MOSFET output capacitance is 0.5. The shunt capacitance is described by

$$C_1 = \frac{C_{j0}}{\sqrt{1+\frac{v_S}{V_{bi}}}} \tag{1}$$

where C_{j0} is the shunt capacitance at the drain to switch voltage $v_S = 0$ and V_{bi} is the built-in potential of the MOSFET body diode.

The transistor is OFF for $0 \le \theta < 2\pi D$, and ON for $2\pi D \le \theta < 2\pi$. While the transistor is OFF, the current through the shunt capacitance is

$$i_C(\theta) = I_{DD} - I_m \sin(\theta + \phi) \tag{2}$$

where I_{DD} is the dc input current, I_m is the output current amplitude, and $\theta = \omega t$. The switch voltage v_S is the integral of the shunt capacitor current i_C given by

$$i_C = C_1 \frac{dv_S}{d\theta}. \tag{3}$$

Integrating both side of this equation with respect of θ gives

$$\omega \int C_1 dv_S = \int i_C d\theta. \tag{4}$$

Substituting C_1 given by (1),

$$\omega\int_0^{v_S}\frac{C_{j0}}{\sqrt{1+\dfrac{v}{V_{bi}}}}dv=\int_0^{\theta}\left[I_{DD}-I_m\sin(\theta'+\phi)\right]d\theta'. \qquad (5)$$

Solving this equation, the switch voltage v_S can be derived as

$$v_S(\theta)=V_{bi}\left\langle\left\{\frac{I_{DD}\theta+I_m[\cos(\theta+\phi)-\cos\phi]}{2V_{bi}\omega C_{j0}}+1\right\}^2-1\right\rangle \qquad (6)$$

3. Circuit Parameters for Optimum Operation at Any Duty Cycle

For the optimum operation,

$$i_C(2\pi D)=0 \qquad (7)$$

and

$$v_S(2\pi D)=0 \qquad (8)$$

are satisfied. Substitution of (7) into (2) yields

$$\phi=\arctan\frac{2\pi D\sin 2\pi D+\cos 2\pi D-1}{\sin 2\pi D-2\pi D\cos 2\pi D}. \qquad (9)$$

Fig. 3 shows ϕ as a function of the duty cycle D. ϕ decreases from positive to negative values as D increases. Substituting (8) into (6),

$$\pi D I_{DD}=I_m\sin\pi D\sin(\pi D+\phi). \qquad (10)$$

Since the power loss in the circuit is zero, the output power is equal to the input power,

$$P_o=I_{DD}V_{DD}=\frac{I_m^2R}{2}. \qquad (11)$$

Substituting (10) into (11), one can obtain the output current amplitude I_m and the output power P_o for the optimum operation at any duty cycle.

$$I_m=\frac{2V_{DD}\sin\pi D\sin(\pi D+\phi)}{\pi DR} \qquad (12)$$

$$P_o=\frac{2V_{DD}^2\sin^2\pi D\sin^2(\pi D+\phi)}{\pi^2D^2R}. \qquad (13)$$

Fig. 4 shows normalized output current amplitude I_mR/V_{DD} and normalized output power P_oR/V_{DD}^2 as a function of the duty cycle D. The normalized output current amplitude I_mR/V_{DD} decreases from 2 to zero as D increases. The normalized output power P_oR/V_{DD}^2 also decreases from 2 to zero as D increases.

Fig. 5 shows $\omega C_{j0}R$ as a function of the duty cycle D and V_{DD}/V_{bi}. $\omega C_{j0}R$ for the optimum operation can be obtained by substituting (9) into

$$\begin{aligned}V_{DD}&=\frac{1}{2\pi}\int_0^{2\pi}v_S(\theta)d\theta\\&=\frac{1}{2\pi}\int_0^{2\pi D}V_{bi}\left\langle\left\{\frac{I_{DD}\theta+I_m[\cos(\theta+\phi)-\cos\phi]}{2V_{bi}\omega C_{j0}}+1\right\}^2-1\right\rangle d\theta\\&=\frac{1}{8\pi\omega^2C_{j0}^2V_{bi}}\left\{\frac{8\pi^2D^3I_{DD}^2}{3}\right.\\&\quad+I_m^2\left[\pi D+\frac{\sin(4\pi D+2\phi)}{4}+2\pi D\cos^2\phi-\sin 2\pi D-\sin(2\pi D+2\phi)+\frac{3\sin 2\phi}{4}\right]\\&\quad\left.+2I_{DD}I_m\left[2\pi D\sin(2\pi D+\phi)+\cos(2\pi D+\phi)-2\pi^2D^2\cos\phi\right]\right\}\\&\quad+\frac{1}{2\pi\omega C_{j0}}\left\{2\pi^2D^2I_{DD}+I_m[\sin(2\pi D+\phi)-2\pi D\cos\phi-\sin\phi]\right\}.\end{aligned} \qquad (14)$$

$\omega C_{j0}R$ reaches the maximum value for $D=0.5$. It increases with an increase in V_{DD}/V_{bi}. The phase angle ϕ_1 of the voltage v_1, i.e., the phase of the sum of the output voltage and the fundamental component of the voltage across the reactance X, is derived as

$$\phi_1=\arctan\frac{b_1}{b_2} \qquad (15)$$

where

$$\begin{aligned}b_1&=\frac{I^2}{4\omega^2C_{j0}^2V_{bi}}\left[\left(4\pi^2D^2-2\right)\sin 2\pi D+4\pi D\cos 2\pi D\right]\\&\quad+\frac{I_m^2}{4\omega^2C_{j0}^2V_{bi}}\left[\frac{\sin 2\pi D}{2}+\frac{\sin(6\pi D+2\phi)}{12}+\frac{\sin(2\pi D+2\phi)}{4}+\cos^2\phi\sin 2\pi D\right.\\&\quad\left.-\frac{\sin 4\pi D}{4}-\pi D-\frac{\sin(4\pi D+2\phi)}{4}-\pi D\cos 2\phi-\frac{\sin 2\phi}{12}\right]\\&\quad+\frac{I_{DD}I_m}{2\omega^2C_{j0}^2V_{bi}}\left[\frac{\pi D\sin(4\pi D+\phi)}{2}+\frac{\cos(4\pi D+\phi)}{8}+\pi^2D^2\cos\phi\right.\\&\quad\left.-2\pi D\cos\phi\sin 2\pi D-\cos\phi\cos 2\pi D+\frac{7\cos\phi}{8}\right]+\frac{I_{DD}}{\omega C_{j0}}(2\pi D\sin 2\pi D+\cos 2\pi D-1)\\&\quad+\frac{I_m}{\omega C_{j0}}\left[\frac{\sin(4\pi D+\phi)}{4}+\pi D\cos\phi-\cos\phi\sin 2\pi D-\frac{\sin\phi}{4}\right],\\b_2&=\frac{I_{DD}^2}{4\omega^2C_{j0}^2V_{bi}}\left[\left(4\pi^2D^2-2\right)\cos 2\pi D-4\pi D\sin 2\pi D+2\right]\\&\quad+\frac{I_m^2}{4\omega^2C_{j0}^2V_{bi}}\left[\frac{\cos 2\pi D}{2}+\frac{\cos(6\pi D+2\phi)}{12}-\frac{\cos(2\pi D+2\phi)}{4}+\cos^2\phi\cos 2\pi D\right.\\&\quad\left.-\frac{\cos 4\pi D}{4}-\frac{\cos(4\pi D+2\phi)}{4}-\pi D\sin 2\phi+\frac{5\cos 2\phi}{12}-\cos^2\phi-\frac{1}{4}\right]\\&\quad+\frac{I_{DD}I_m}{2\omega^2C_{j0}^2V_{bi}}\left[\frac{\pi D\cos(4\pi D+\phi)}{2}-\frac{\sin(4\pi D+\phi)}{8}+\pi^2D^2\sin\phi\right.\\&\quad\left.-2\pi D\cos\phi\cos 2\pi D+\cos\phi\sin 2\pi D+\frac{\sin\phi}{8}\right]+\frac{I_{DD}}{\omega C_{j0}}(2\pi D\cos 2\pi D-\sin 2\pi D)\\&\quad+\frac{I_m}{\omega C_{j0}}\left[\frac{\cos(4\pi D+\phi)}{4}+\pi D\sin\phi-\cos\phi\cos 2\pi D+\frac{3\cos\phi}{4}\right].\end{aligned}$$

Fig. 6 shows X/R as a function of the duty cycle D and V_{DD}/V_{bi}. X/R can be obtained by substituting (9) into (15). X/R increases with an increase in the duty cycle D, but it does not change significantly with a change in V_{DD}/V_{bi}. Fig. 7 shows normalized peak switch voltage V_{SM}/V_{DD} versus duty cycle D and V_{DD}/V_{bi}. V_{SM}/V_{DD} increases from zero to a positive value as the duty cycle D is increased from 1 to zero. Fig. 8 shows

power output capability c_p versus duty cycle D and V_{DD}/V_{bi}. c_p is obtained as

$$c_p = \frac{P_0}{I_{SM} V_{SM}}. \qquad (16)$$

where P_o is the output power of the optimum operation, I_{SM} is the peak switch current for the optimum operation, which is obtained by substituting (12) into (2), and V_{SM} is the peak switch voltage for the optimum operation, which is obtained as $v_S(\theta_1)$ in which θ_1 is obtained from (6). c_p is maximum when $D = 0.5$. c_p does not change much with a change in V_{DD}/V_{bi} when $V_{DD}/V_{bi} > 5$.

4. Simulation Results

The example circuit was simulated with PSpice. The circuit parameters were $V_{DD} = 10\,\text{V}$, $L_{RFC} = 100\,\mu\text{H}$, $C = 9.77\,\text{nF}$, $L = 3.18\,\mu\text{H}$, $R = 2\,\Omega$. The operating frequency was 1 MHz. The duty cycle was 0.6. The SPICE MOSFET MODEL Level 3 was used for the MOSFET. In the SPICE MOSFET model, the drain-source capacitance is expressed as [4]

$$C_1 = \frac{\text{CBD}}{\left(1 + \frac{v_S}{\text{PB}}\right)^{\text{MJ}}}, \qquad (65)$$

where CBD is the zero-bias bulk-junction capacitance, which is the same as C_{j0}, PB is the bulk junction potential which is the same as V_{bi}, and MJ is the bulk bottom grading coefficient which is 0.5 in this example. In accordance with the calculations, we set CBD = 65 nF, PB = 0.7 V, and MJ = 0.5.

The simulated waveforms of switch voltage v_S and the output voltage v_o are shown in Fig. 9. The peak switch voltage V_{SM} was 32.5 V (36 V in theory). The output voltage amplitude V_m was 6.35 V (7.66 V in theory). In our design, the MOSFET on-resistance and the gate-drain capacitance were ignored. The existence of these parasitic components may cause errors.

References

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[4] R. M. Kielkowski, *SPICE Practical Device Modeling*, New York: McGraw-Hill Inc., 1995, Chapters 3 and 6.

[5] C. H. Li and Y. O. Yam, "Maximum frequency and optimum performance of Class E amplifiers," *IEE Proceedings,Circuits, Devices and Systems*, vol. 141, pp. 174-184, 1994.

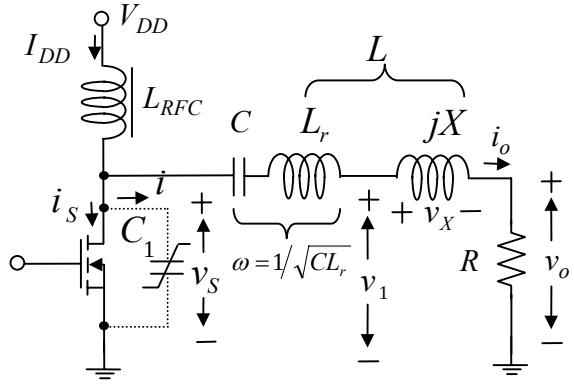

Fig. 1. Basic circuit of a class E amplifier.

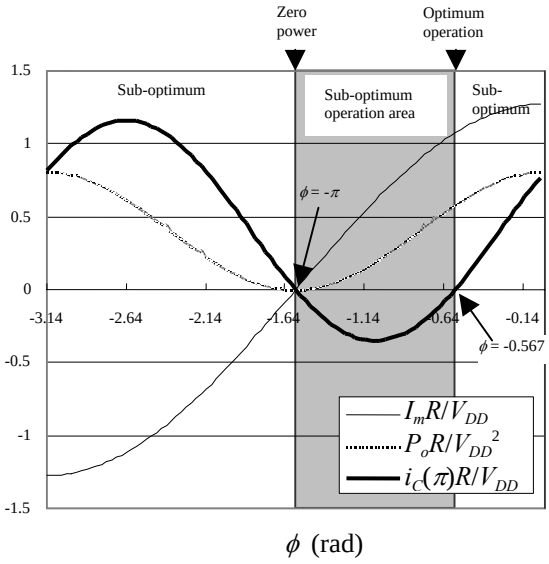

Fig. 2. Normalized output current amplitude I_mR/V_{DD}, normalized output power P_oR/V_{DD}^2, and normalized shunt capacitance current at switch turning-on $i_C(\pi)R/V_{DD}$ as functions of ϕ.

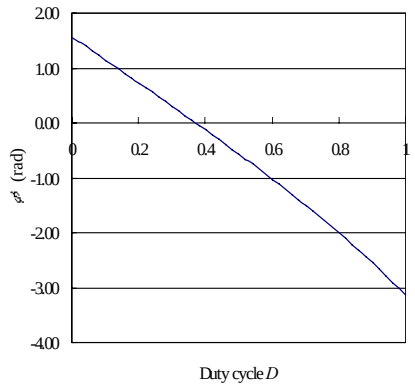

Fig. 3. Phase angular ϕ versus duty

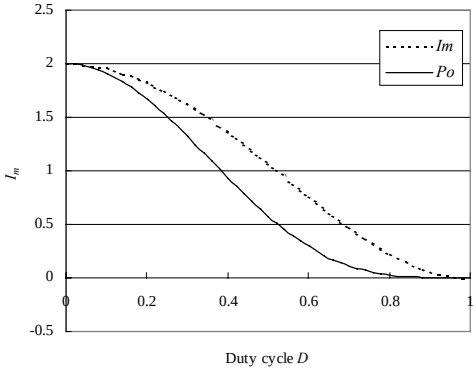

Fig. 4. Normalized output current amplitude $I_m R / V_{DD}$ and normalized output power $P_o R / V_{DD}^2$ versus duty cycle D.

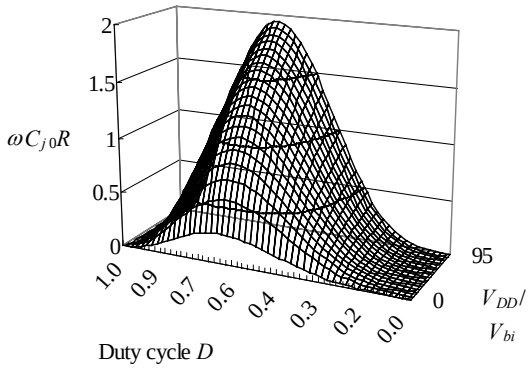

Fig. 5. $\omega C_{j0} R$ versus duty cycle D.

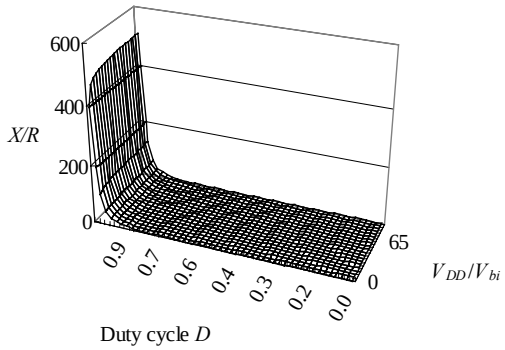

Fig. 6. X / R versus duty cycle D.

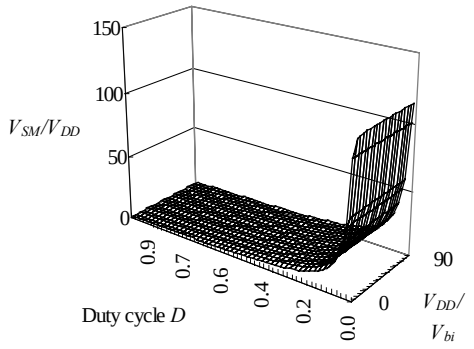

Fig. 7. Normalized peak switch voltage V_{SM} / V_{DD} versus duty cycle D and V_{DD} / V_{bi}.

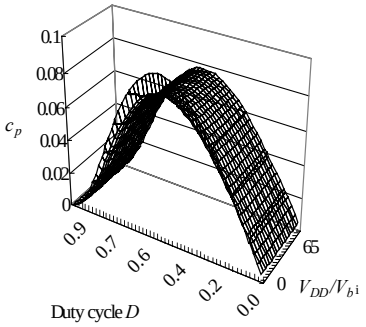

Fig. 8. Power output capability c_p versus duty cycle D and V_{DD} / V_{bi}.

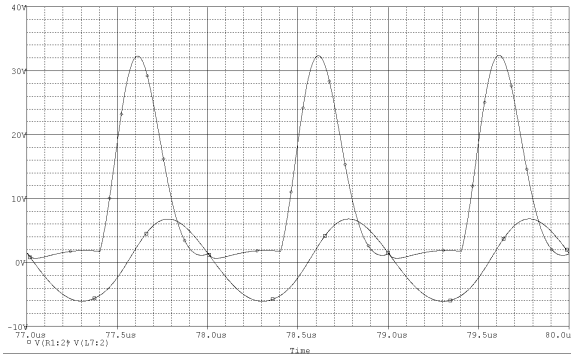

Fig. 9. Simulated waveforms of the switch voltage v_S and the output voltage v_o.