

## Bifurcations in a Boost PFC Circuit Under Different Control Strategies

A. El Aroudi<sup>†</sup>, M. Orabi<sup>‡</sup>, L. Martínez-Salamero<sup>†</sup> and T. Ninomya<sup>◊</sup>

<sup>†</sup>Departament d'Enginyeria Electrònica, Elèctrica i Automàtica, Universitat Rovira i Virgili  
Tarragona, Spain, aearoudi@etse.urv.es

<sup>‡</sup>Dept. of Electrical Eng. , Faculty of Engineering, South Valley,  
University, Aswan, Egypt, orabi@ieee.org.

<sup>◊</sup>Dept of EESE, Graduate School of ISEE, Kyushu  
University, Fukuoka 812-8581, Japan, ninomiya@ees.kyushu-u.ac.jp, Japan

**Abstract**—Different bifurcation phenomena are studied for a Boost Power Factor correction (PFC) circuit under three different control strategies. Fixed Frequency Averaged Current Control (FFACC), Variable Frequency Averaged Current Control (VFACC) and Fixed Frequency Averaged Current Control (FFACC) are used. A new bifurcation phenomenon called slow scale instability at the line frequency is discovered and analyzed by using nonlinear averaged modeling approach. Other kinds of bifurcation like the fast scale instability at both the switching and the line frequency are also possible. Some guidelines for an optimized stable design and a power factor close to one are outlined.

### 1. Introduction

The quality of the current absorbed from the utility line by electronic equipments is attracting many researchers over the world [1, 3]. Many efforts were devoted to improve the power factor of standard electronic loads by using Power Factor Correction (PFC) circuits. These systems must draw a sinusoidal input current from the line source. In order to do it a control circuit should shape the input current to follow as close as possible a suitable sinusoidal current reference. The most popular circuit used for this purpose is the well known boost Power Electronic (PE) converter with current mode control. PE circuits are nonlinear systems due to the switching action and feedback loop. Recently a great variety of complex nonlinear behaviors are shown to be possible in even simple PE circuits like buck, boost and buck-boost DC-DC converters [2]. Nonlinear analysis can be extended to other more complex circuits like PFC circuits. These circuit are more complex in the sense that their dynamics are characterized naturally by two different frequencies and therefore by two different scales of time. Many works are devoted to the characterization of the nonlinear behavior of boost PFC circuit and different kinds of instability phenomena were detected. In [3], period doubling phenomena is observed at the line frequency

which was called slow scale instability while in [4] the same behavior is observed at the switching frequency which was called fast scale instability. Theoretically, other kinds of instability are possible like Hopf bifurcation at the line frequency and Hopf bifurcation at the switching frequency. In practice, the switching frequency is much greater than the line frequency in such a way that Hopf bifurcation at the line frequency is slow scale instability for both the switching and line frequency while Hopf bifurcation at the switching frequency is a slow scale instability at the switching frequency but it can be fast scale instability at the line frequency. All these instabilities depend the value of parameters used. Traditionally, there are many control strategies to control these systems. For the sake of brevity we will apply three different controllers to the system and their dynamics will be characterized by using nonlinear averaged and discrete time model. The controllers studied in this work are:

1. Fixed Frequency Peak Current Control (FFPCC)
2. Variable Frequency Average Current Control (VFACC) or Hysteretic Control (HC)
3. Fixed Frequency Average Current Control (FFACC)

Figure 1 shows the block diagrams for each of the controllers used in this paper. The control objectives in the PFC circuit are to guarantee that the inductor current be in phase with the input voltage in order to ensure a power factor close to one and to drive the output voltage towards a desired constant level. As the power stage circuit is a non minimum phase system when the capacitor voltage is the output variable, different instability phenomena can occurs in this system. Theoretically, as the system has two forcing periods, bifurcation phenomena can occur at different scale of time. The present paper deals with studying these bifurcation phenomena in a boost PFC circuit under the three different controllers mentioned previously. These

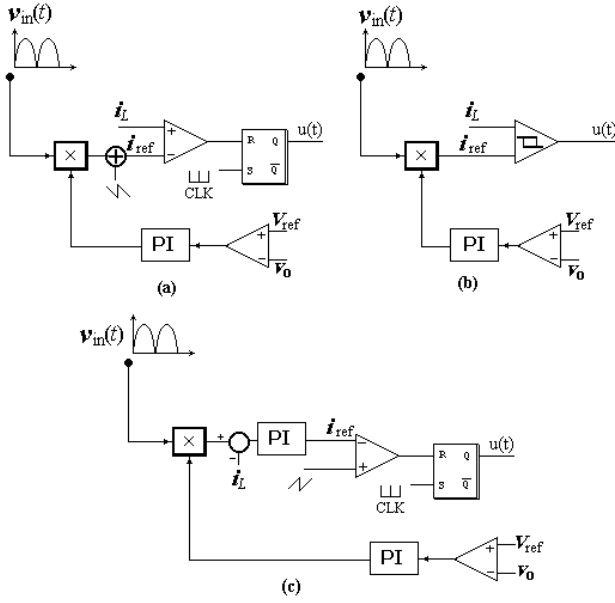


Figure 1: Block diagrams of (a) FFPCC, (b) VFACC and (c) FFACC

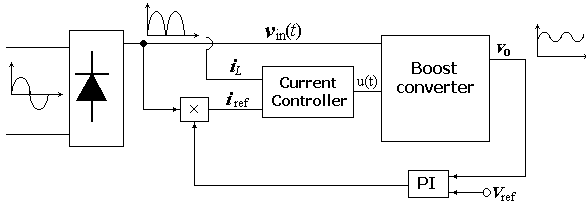


Figure 2: Block diagram of a boost PFC circuit

phenomena are discovered first by simulating the system from its exact circuit diagram and then by using its large signal nonlinear averaged model. Some guidelines for an optimized design and a high power factor are outlined. Traditionally, it was assumed that the output capacitor is sufficiently large in such a way that the output voltage is constant. The system is then linearized near an operating point and the stability of the system is studied by using linear techniques. Instead, in this paper, we will use a nonlinear model of the system. We will show that a very large capacitor can give rise to undesired bifurcation phenomena.

## 2. Slow Scale Instability at the Line Frequency from the Circuit Diagram

A schematic diagram of a PFC boost AC-DC converter is shown in Fig. 2. The circuit is designed in order to give periodic waveforms of both output capacitor voltage and inductor current. There are two periods that characterize the dynamics of the system,

the switching period  $T_s$  and the line period  $T_o$ . Typical waveforms of the state variables and the rectified input voltage are shown in Fig. 3. The value of the circuit parameters used in this figure are: amplitude of the input voltage  $V_{in} = 220\sqrt{2}$  V, line frequency  $f = 60$  Hz, desired averaged output voltage  $v_o = V_{ref} = 500$  V, output capacitor  $C = 10$  mF, load resistance  $R = 100$   $\Omega$ , inductance of the inductor  $L = 5$  mH. The controller used is VFACC with the value of the PI controller parameters of the voltage loop are: gain coefficient of the PI controller  $k_1 = 0.001$  and its time constant  $\tau_1 = 0.001$  s. The hysteresis width is  $h = 1$ . In this paper slow scale instability means Hopf bifur-

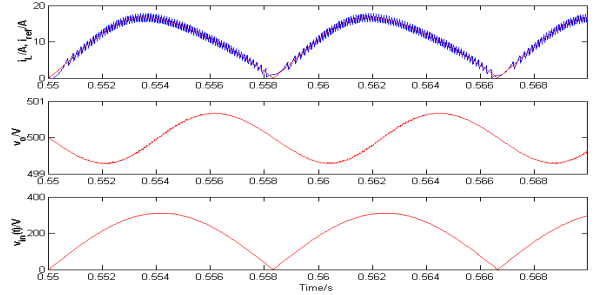


Figure 3: Typical waveforms in normal operation of a PFC boost converter

cation and the term ‘at the line frequency’ means that after Hopf bifurcation takes place a frequency less than the line frequency appears in the dynamics of the system and the attractor is a torus  $T^3$ . The torus is tri-dimensional because the dynamical behavior of the system contains three different frequency: the switching frequency, the line frequency and a lower frequency which appears after Hopf bifurcation takes place. Figure 4-a shows the state variables of the PFC boost converter controlled by a VFACC strategy showing a slow scale instability at the line frequency. The same behavior is shown in Fig. 4-b for a FFACC system. Note the value of the capacitor voltage is very large. In fact, this is the main cause of the slow scale instability at the line frequency in this system.

## 3. Fast Scale Instability at the Line Frequency from the Circuit Diagram

Fast scale instability means period doubling bifurcation and the term ‘at the line frequency’ means that after this bifurcation takes place the period of the system is twice the period of the rectified line voltage. Figure 5-a shows the state variables of the PFC boost converter controlled by a FFPCC strategy showing a fast scale instability at the line frequency. The same behavior is shown in Fig. 5-b for a VFACC system. FFACC system can present the same behavior and it is not shown here for space limitation.

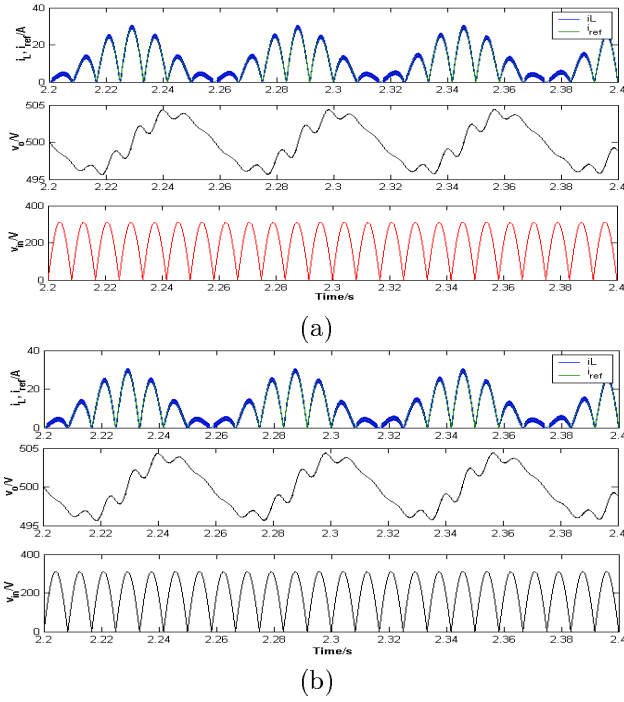


Figure 4: Typical waveforms showing slow scale instability at the line frequency (a) VFACC with control parameters  $k_1 = 0.00012$  and  $\tau_1 = 0.0001$  s, (b) FFAPCC with control parameters  $k_1 = 0.00012$  and  $\tau_1 = 0.0001$  s,  $k_2 = 4$ ,  $\tau_2 = 0.001$  s

#### 4. Fast Scale Instability at the Switching Frequency from the Circuit Diagram

A very common and well known bifurcation phenomenon in power electronic DC-DC converters is the subharmonic instability or period doubling bifurcation at the switching frequency. In an AC-DC power factor circuit, the line voltage is assumed to vary very slowly with respect to the clock signal in such a way that both reference signal and input voltage can be considered constant during a switching cycle. Subharmonic instability or the so called fast scale instability at the switching frequency is also possible in this case. This phenomenon was first discovered in [4]. Figure 6-a shows the state variables of the PFC boost converter controlled by a FFPC strategy showing a fast scale instability at the switching frequency. The same behavior is shown in Fig. 6-b for a FFACC system. It should be noted that this behavior is not detected in the FFACC system.

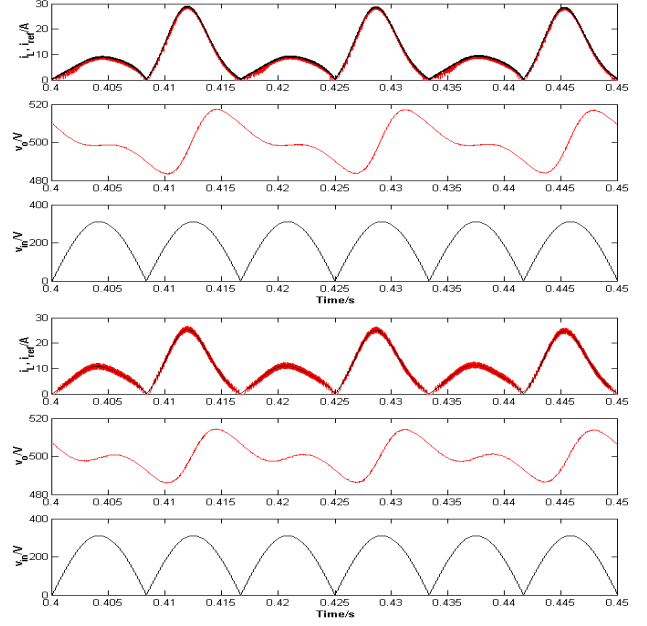


Figure 5: Typical waveforms showing fast scale instability at the line frequency (a) FFPCC with control parameters  $k_1 = 0.00101$  and  $\tau_1 = 0.001$  s, switching frequency 20 kHz and amplitude of the ramp signal 0.4 A, (b) VFACC with control parameters  $k_1 = 0.00101$  and  $\tau_1 = 0.001$  s and hysteresis width  $h = 2$  A. The capacitance of the capacitor is 1 mF.

## 5. Bifurcation Phenomena Obtained from the Averaged Model

### 5.1. Slow scale instability at the line frequency for the VFACC and FFACC system

Figure 7 shows the waveforms of the averaged state variables showing a fast scale instability at the line frequency for the VFACC and FFACC cases. Comparing with Fig. 4, it can be observed that, there is a good concordance between the results obtained from the averaged model and those obtained from the exact switched circuit diagram.

### 5.2. Fast scale instability at the line frequency for the VFACC and FFACC system

The fast scale instability at the line frequency like that studied in [3] can be detected by using the same model. Figure 8 shows the waveforms of the averaged state variables showing a fast scale instability at the line frequency for the VFACC and FFACC cases. Comparing with Fig. 5, it can be observed again, that the results match well with those obtained from the switched model. However we can see that the fast scale instability at the switching frequency can not be detected by using the averaged model. This requires a discrete time modeling approach.

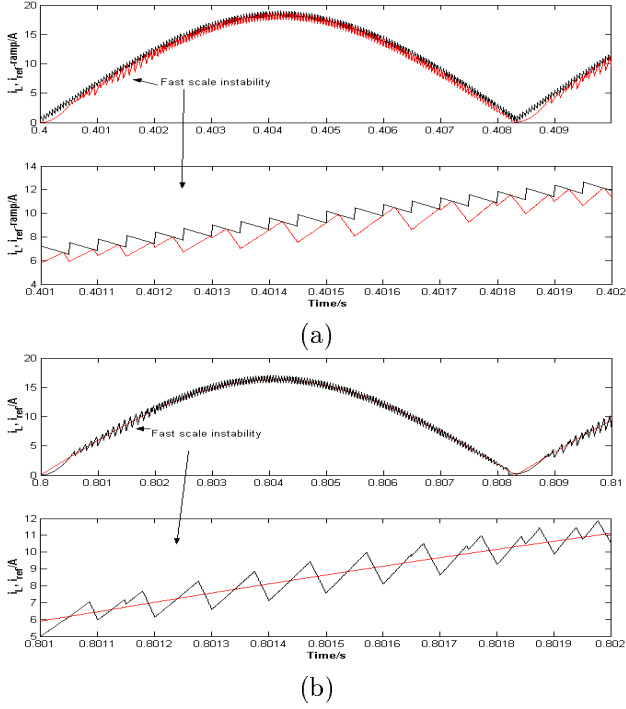


Figure 6: Typical waveforms showing fast scale instability at the switching frequency (a) FFPCC with control parameters  $k_1 = 0.001$  and  $\tau_1 = 0.001$  s, amplitude of the ramp signal 1 A, capacitor voltage  $C = 10$  mF and the remaining parameters as before, (b) FFACC with control parameters  $k_1 = 0.001$  and  $\tau_1 = 0.001$  s,  $k_2 = 1$ ,  $\tau_2 = 0.001$  s, amplitude of the ramp signal 1 A, capacitor voltage  $C = 10$  mF and the remaining parameters as before.

## 6. Analysis of Fast Scale Instability at the Switching Frequency

A discrete-time modeling approach most commonly comes from regular sampling of the state variables of the continuous-time description. Because the majority of power circuits operate cyclically, this model is the more accurate one in predicting the different kinds of instabilities of these systems. As discrete-time modeling approach is a natural way to represent the periodic behavior of PE converters, this approach does not assume the approximations taken in averaged modeling approach. To build-up the discrete-time model of a PE circuit, we consider the operation of the system within the  $n$ th cycle. For PE circuits, the system configuration during each switching sub-interval is linear and closed form expressions for the solutions are available. These can be cascaded at the switching instants and the map  $P$  which relates two successive samples of the state variable is obtained. For a PFC circuit, there are two kinds of discrete time models, one describing the dynamical behavior of the system along the switching cycle and the other one describing the

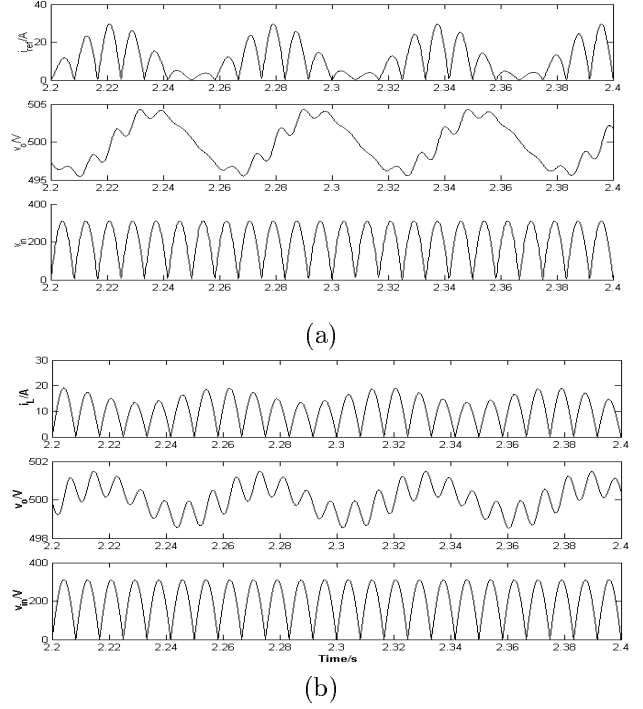


Figure 7: Typical waveforms showing slow scale instability at the line frequency obtained from the averaged model, (a) VFACC, (b) FFACC. The parameter used are the same as in Fig. 4

dynamics along the line cycle. In this section we study the local dynamics during the switching cycle and in a future work we will present results by using the global second order Poincaré map. In continuous conduction mode there are two and only two configurations during a switching cycle. The duration of this cycle may be fixed (FFACC) and (FFPCC) or variable (VFACC). The system switches cyclically among 2 linear configurations during this cycle. In order to simplify the analysis, we use the fact that the switching frequency is much higher than the line frequency in such way that during a switching cycle, the input voltage and hence the reference current are practically constant. It should be noted that for FFACC and FFPCC systems the sampling duration  $T_n$  is constant and it is equal to the period of the clock signal while for VFACC this duration is variable from cycle to cycle. The mapping that relates the state variable  $x_n$  at the beginning of an entire cycle to  $x_{n+1}$ , those at the end of the same cycle, can be expressed in the following way:

$$P : \Sigma \mapsto \Sigma$$

$$x_n \mapsto x_{n+1} := P(x_n, T_n, t_n) \quad (1)$$

For FFACC and FFPCC system and under stroboscopic sampling,  $T_n = T$  is known, where  $T$  is the period of the clock signal. In this case, only one switching equation is therefore to be solved to obtain  $t_n$ . But

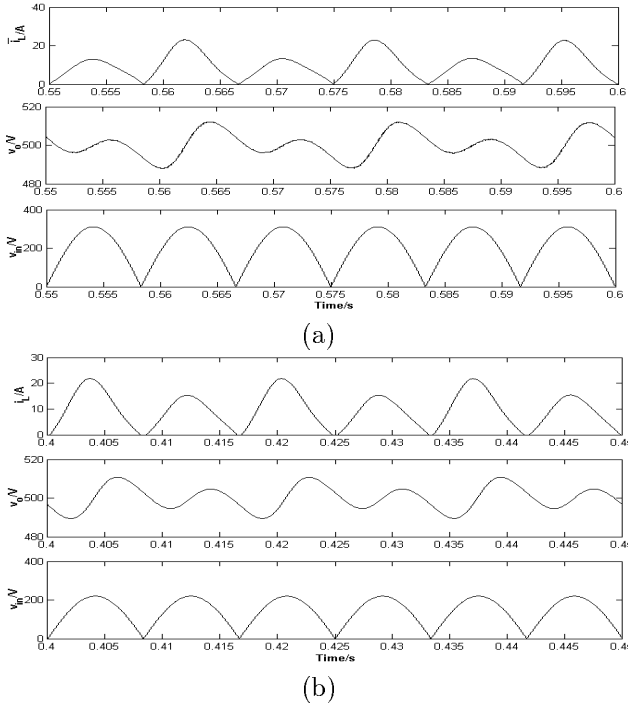


Figure 8: Waveforms of the state variables showing fast scale instability at the line frequency frequency obtained from the averaged mode and using the same value of parameters in Fig. 4, (a) VFACC system, (b) FFPCC system

in the case of VFACC system,  $T_n$  is variable and unknown and two switching equations are to be solved to obtain  $t_n$  and  $T_n$ . The general switching equation may be written in the following form:

$$\sigma(x_n, t_n, T_n) := \begin{bmatrix} \sigma_1(x_n, t_n) \\ \sigma_2(x_n, t_n, T_n) \end{bmatrix} \quad (2)$$

The map (Eq. (1)) and the constraint (Eq. (2)) define a generalized discrete-time model for boost PFC circuit with two configurations and under the different control strategies. The fixed point of  $P$  can be obtained by enforcing the periodicity:  $x_n = x_{n+1} = x^*$ . Using the expression of  $P$ ,  $x^*$  can be expressed in terms of switching time  $t_n$  and system transition matrices. In general, the solution of the equation  $\sigma(\tau^*, T^*) = \mathbf{0}$  is not available in closed form. Therefore a root finding algorithm should be applied. Once the fixed points are located, their stability analysis may be carried out by studying the local behavior of the map  $P$  near these fixed points. The small signal model for the discrete time model can be written as:

$$\tilde{x}_{n+1} \approx DP(x^*)\tilde{x}_n \quad (3)$$

where  $DP$  is the Jacobian matrix whose eigenvalues  $\lambda_i$  of  $DP$  which are also called the *characteristic* give the amount of expansion or contraction near the fixed

point  $x^*$  when the map is once iterated. Therefore they determine the stability of the fixed point and hence of its underlying periodic orbit. A sufficient condition for stability is that all characteristic multipliers lie inside the unit circle. Evaluating the Jacobian matrix  $DP$  in a fixed point and computing its corresponding characteristic multipliers  $\lambda_i$  would give us the stability of its underlying periodic orbit. If  $DP$  has all eigenvalues within the unit circle, the periodic orbit is stable. If an eigenvalue crosses the unit circle from inside to outside, the periodic orbit loses its stability and this is a sign of a bifurcation. In the remainder of this paper when we talk about a bifurcation of an orbit, we refer to nominal orbit which is characterized by 2 switching instants per switching cycle. In a Boost PFC circuit the main varying parameter is the input voltage  $v_{in}$  and it can be considered as a bifurcation parameter. However, this parameter changes from a null value to a maximum value given by the amplitude of the sinusoidal voltage ( $220\sqrt{2}$  in our case). The parameter  $i_{ref}$  is also zero when  $v_{in}$  is. It can be shown that for  $i_{ref} < v_{in}/R$  system present no periodic behavior. In this case the system evolves to an equilibrium point which depends on the input voltage and which varies from cycle to cycle. This is the main cause of distortion of the input current that make the power factor to be far from 1. When  $i_{ref} > v_{in}/R$ , the condition for periodicity is fulfilled. If the nominal periodic orbit during one switching cycle is stable, the dynamics during this cycle is periodic orbit. But it can be subharmonic or even chaotic if the stability of the nominal periodic orbit is not assured. Traditionally the slope of the ramp voltage is adjusted in order to ensure stability for DC-DC converters in the operating point. The problem with the PFC boost AC-DC converter is that this operating point is time varying. However we can select the value of the slope of the ramp for the worst operating case which corresponds to a null value of the input voltage. It can be demonstrated that using a slope  $m_c = Vref/2L$ , the stability can be assured during the whole range of the input voltage.

For the sake of brevity we present the results corresponding to the VFACC and FFPCC system only. The same procedure can be used for the other case. As it was already mentioned the VFACC system subharmonic oscillation at the switching frequency were not detect for the set of parameter values used in this paper. Figure 9-a shows a set of stationary waveforms of the VFACC system during one switching period obtained from the discrete time approach by varying the input voltage in the range  $(60\sqrt{2}, 220\sqrt{2})$ . The location of the eigenvalues of the Jacobian matrix of the discrete time model is also shown indicating stability for whole range of the input voltage. Observe that in this case the duration of the switching cycle varies. Figure 9-b shows stationary waveforms of the FFPCC

system during one switching period by varying the input voltage in the same range. In the case of FFPC, we observe that at critical value of the input voltage one of the eigenvalues is equal to -1 indicating a flip bifurcation which give rise to subharmonic bifurcation and chaos. It should be noted that all the results are obtained assuming a constant value of the input voltage during a switching cycle. However, in a real PFC circuit the input voltage can be supposed to vary linearly from cycle to cycle. During the first half period of the line cycle, the input voltage is increasing and its slope is positive while it is decreasing during the second half period and its slope is negative. A more accurate analysis should take into account the variation of the slope of the input voltage during one line cycle and the change of its sign. This explains the asymmetry observed in the critical points at which the first bifurcation occurs (see Fig. 6). This was studied and explained in details in [4]

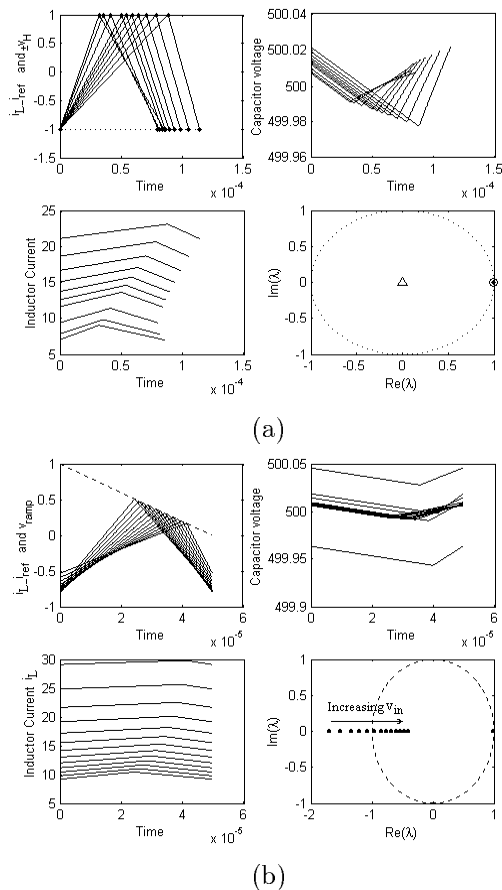


Figure 9: Stationary waveforms of the system during one switching period obtained from the discrete time approach, (a) VFACC system. Parameter values hysteresis width 1 A,  $k_1 = 0.001$  and  $\tau_1 = 0.001$  (b) FFPC system. Parameter values The switching period  $T = 50 : \mu s$ , amplitude of the ramp voltage 1 A and its lower value zero,  $k_1 = 0.001$  and  $\tau_1 = 0.001$

## Conclusions

Different bifurcation phenomena are detected and studied for an AC-DC boost PFC circuit under different control strategies. Three different controllers are applied to the system and it was shown that they can give rise to similar averaged behavior. These are FFPC, FFACC and VFACC. A new bifurcation phenomenon, so called slow scale instability at the line frequency, is discovered from the circuit diagram and the analytical large signal averaged model. Slow scale instability and fast scale at the line frequency is possible in all cases. Fast scale instability at the switching frequency is not detected for the VFACC while it is observed in the other two cases. A discrete time approach is required to detect this instability phenomenon. Such a discrete time representation of the system dynamics is presented here in a generalized framework.

It can be claimed that in order to obtain a good power factor correction the feedback gains should not be large. But an excessively small value of the feedback coefficient of the PI controller and its time constant can give rise to the new detected phenomenon. In the other hand, stable operation does not mean always a good power factor correction. Some times the dynamics of the system is periodic but this factor is very low. Further study will deal with analyzing the bifurcation phenomena by using Floquet theory and harmonic balance. Some phenomena which are not reported here like coexistence of attractors are observed and it requires a more detailed analysis. Experimental confirmation of some new phenomena is also the subject of future work.

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