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Neuromorphic Single-Electron Circuit and its Application to Temporal-Domain Neural Competition

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Abstract—We propose neuromorphic single-electron circuits for fundamental neural components in modern spiking neural networks, aiming at implementing artificial neural networks on a single or multi-layer nano-dot array. A unit circuit consists of a pair of single-electron oscillators. Using these unit circuits with coupling capacitors, we designed a single-electron neuron circuit that consists of excitable axons and dendrites, excitatory and inhibitory synapses, and a soma. We present an application of the neuron circuit in an inhibitory neural network, where the neurons compete with each other in the temporal domain.

1. Introduction

Quantum and molecular electronics are expected to push advances in future VLSI technology far beyond the limits of silicon CMOS technology. However, robust and fault-tolerant circuit architectures for nano-devices and single-electron devices are necessary for designing practical quantum LSIs because conventional computing methodologies for CMOS devices cannot be used for nano-devices, due to their uncertainty. Unconventional computing architectures for nano-devices are thus required. A neural network is one of the primary components for such an architecture.

Likharev *et al.* recently proposed novel neuromorphic concepts for hybrid VLSIs that combine a layer of advanced CMOS devices for neurons with two mutually perpendicular arrays of parallel nanowires for axons and dendrites [1]. Here, we propose neuromorphic circuits for a *nano-dot array* (See Fig. 1) that has already been fabricated [2]. Our neuron circuit consists of excitable axons and dendrites, excitatory and inhibitory synapses, and a soma. Since our synapse circuit cannot store connection weights between neurons at present, neural networks with no variable weights, or, networks in which weights are represented by dynamics, will be best suited to the circuit's application. As an example, we used an inhibitory competitive neural network that had been implemented on CMOS VLSIs [3]. We demonstrate basic operation of the proposed devices and their competitive performance through circuit simulations. We considered the noise-tolerance of the network, and discuss possible implementation of the proposed circuits in this paper and future synaptic memory devices using single-electron circuits.

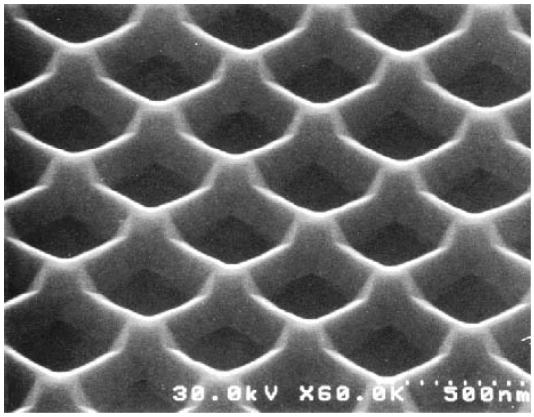

Figure 1 Micrograph of nano-dot array [2].

2. Single-Electron Circuits for Spiking Neuron Models

To produce action potentials on a nano-dot array (Fig. 1), we propose the use of an excitable single-electron tunneling (SET) oscillator [shown in Fig. 2(a)]. The oscillator consists of a tunneling junction (C_i), a resistive device (R), and a bias voltage source ($V_{\rm dd}$). The oscillator has an island node n_i where excess electrons are stored. Figure 2(b) is a nominal phase diagram of this circuit for positive $V_{\rm dd}$. The vertical and horizontal axes represent node voltage n_i and a tunneling phenomenon [= 1 (when an electron tunnels), 0 (else)] at C_i. Note that trajectories between the tunneling phenomenon (0 and 1) in the figure do not have any quantitative physical meaning but have been used only to explain this circuit's operation. We have assumed that $V_{\rm dd} < e/2C_i$ ($\equiv V_{\rm T}$: tunneling threshold voltage of junction C_i). Since tunneling junction C_i is charged by $V_{\rm dd}$ [(i) in Fig. 2(b)], the circuit is stable when $n_i = V_{\rm dd}$. Under this resting condition, if n_i is further increased by an external input and exceeds $V_{\rm T}$, an electron tunnels from the ground to node i through junction C_i, which results in the sudden decrease of n_i from $V_{\rm T}$ to $-V_{\rm T}$ [(ii) in Fig. 2(b)]. Then $V_{\rm dd}$ starts charging C_i and the circuit become stable again [(i) in Fig. 2(b)]. Note that there is a time lag from when the junction voltage exceeds $V_{\rm T}$ to when tunneling actually occurs. We utilized this "monostable" (excitable) oscillatory property to produce action potentials in spiking neural networks.

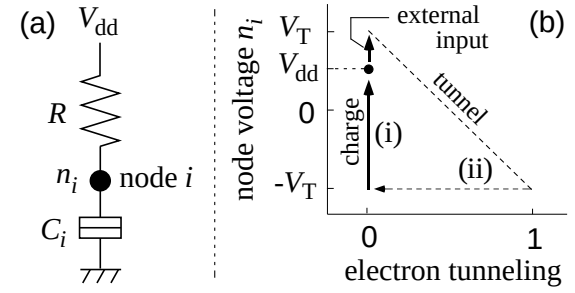

Figure 2 Single-electron oscillator and phase diagram.

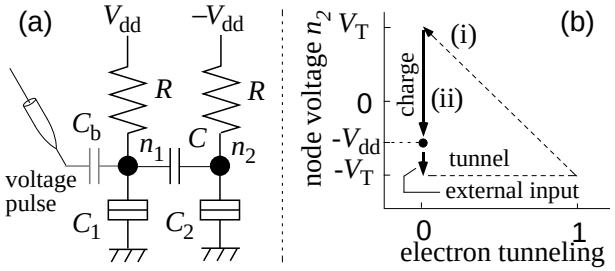

Figure 3 Unit circuit for single-electron neuron circuit.

To propagate action potentials on a nano-dot array, we used a chain of monostable single-electron oscillators. Figure 3(a) shows a unit circuit where two single-electron oscillators are connected laterally through a coupling capacitor (C). They are biased by positive ($V_{\rm dd}$) and negative supply voltages ($-V_{\rm dd}$). External input is a voltage pulse and is applied to the unit circuit through a buffering capacitor ($C_{\rm b}$). Figure 3(b) is a nominal phase diagram of a single-electron oscillator biased by negative supply voltage $-V_{\rm dd}$. The unit circuit becomes stable when $n_1 = V_{\rm dd}$ and $n_2 = -V_{\rm dd}$. Under this resting condition, by applying a pulse voltage that makes $n_1 \geq V_{\rm T}$, n_1 is suddenly decreased to -$V_{\rm T}$ and junction C_1 is then charged up to $n_1 = V_{\rm dd}$. This sudden decrease in n_1 also decreases n_2 because of coupling capacitance C. If this sudden decrease makes $n_2 \leq -V_T$, an electron tunnels from node 2 to the ground through junction C_2, which results in a sudden increase of n_2 from $-V_{\rm T}$ to $V_{\rm T}$ [(i) in Fig. 3(b)]. Then $-V_{\rm dd}$ starts charging C_2 and the circuit become stable again [(ii) in Fig. 3(b)]. Consequently, electron tunneling at junction C_1 triggered by the external voltage pulse is transmitted to subsequent electron-tunneling at junction C_2. Therefore, if we connect several unit circuits serially as can be seen in Fig. 4 (open and closed circles represent island nodes biased by positive and negative voltages, respectively), an electron-tunneling "phenomenon" is transmitted throughout the array.

Our axon and dendrite circuits are bidirectional spike-transmission devices. Again, we assumed that a soma would accept spike trains from dendrites and transfers their sum to the axon. The soma is thus not a bidirectional transfer device but should be unidirectional. Figure 5 illustrates our unidirectional soma circuit coupled with single-

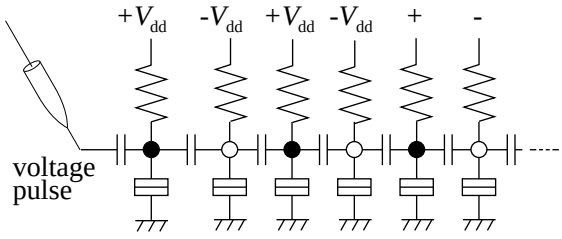

Figure 4 Single-electron axons and dendrites.

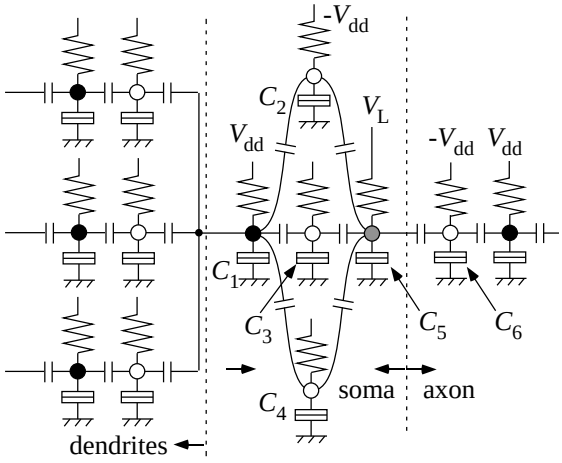

Figure 5 Single-electron neuron circuit.

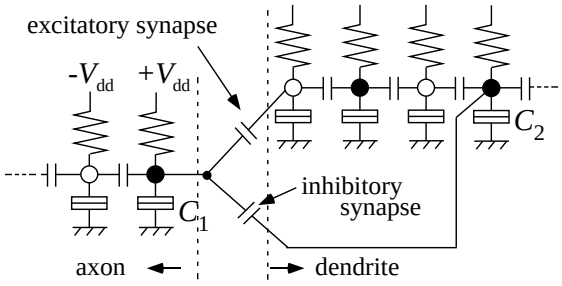

Figure 6 Single-electron synapse circuits.

electron dendrites and axons. Action potentials from dendrites lead to electron tunneling at junction C_1, which results in subsequent electron tunneling at junctions C_2, C_3, and C_4. Junction C_5 is biased by positive voltage $V_{\rm L}$ so that electron tunneling at C_5 is not evoked by a single oscillator but multiple oscillators; e.g., 3 oscillators in Fig. 5. Therefore, simultaneous electron tunneling at 3 junctions (C_2, C_3, and C_4) leads to electron tunneling at C_5. Action potentials from dendrites are therefore transmitted to the axon. Action potentials from the axon, on the other hand, do not lead to electron tunneling at C_5 because electron tunneling at only one junction (C_6) cannot evoke subsequent tunneling at C_5.

Figure 6 is a diagram of the single-electron synaptic circuit we propose. The circuit connects dendrites and axons with fixed weight strength (developing a variable weight-storage circuit is another subject altogether). Excitatory and inhibitory synapses are thus represented by coupling

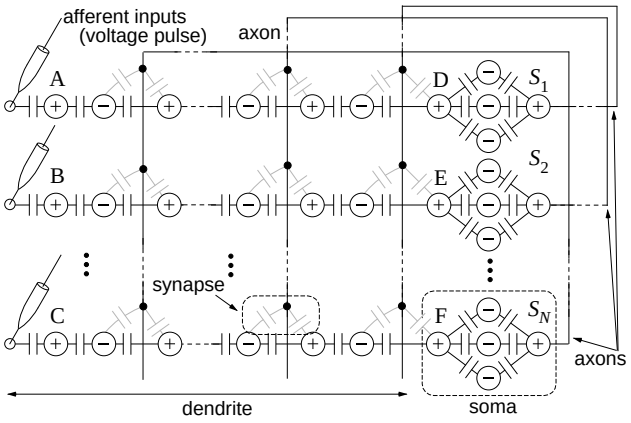

Figure 7 Single-electron inhibitory network for temporal-domain neural competition.

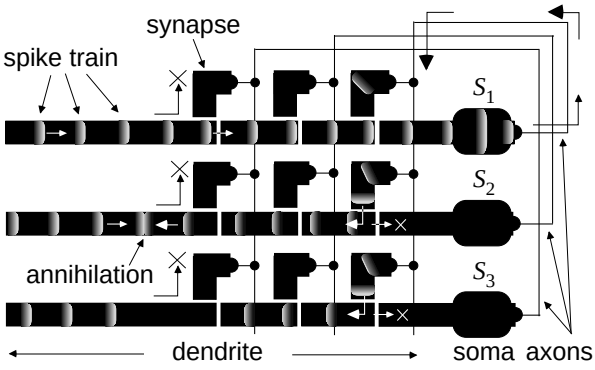

Figure 8 Signal flows of spike trains in single-electron network.

capacitors between axons and dendrites. If an oscillator biased by negative (or positive) voltage in an axon circuit is coupled with the other oscillator biased by positive (or negative) voltage in a dendrite circuit, spike trains in axons are transmitted to dendrites. However, spike trains in dendrites are blocked (inhibited) when an oscillator biased by negative (or positive) voltage in axon circuits is coupled with the other oscillator biased by negative (or positive) voltage in dendrites. For example, electron tunneling at C_1 in Fig. 6 blocks spike trains on dendrites at C_2 because both node voltages of C_1 and C_2 are decreased by tunneling at C_1, which prevents subsequent electron tunneling at C_2.

3. Application of Neuromorphic Single-Electron Circuits to Temporal-Domain Neural Competition

To demonstrate our single-electron neuron circuits, we constructed an inhibitory neural network in which the neuron circuits are coupled to each other through all-to-all inhibitory connections of equal strength. Afferent inputs were encoded as spike timing. Encoding the input as spike-timing code meant that the strength was equivalent to the timing of spike generation relative to the timing of its external periodic input.

Figure 7 shows the inhibitory neural network consisting of N neurons and N^2 synapses, where $\oplus$ and $\ominus$ represent single-electron oscillators biased by positive and negative voltages. Afferent inputs (voltage pulses) are applied at the end of dendrites. Each soma circuit accepts spike trains from dendrites. In the figure, axons are represented by wires instead of transmission circuits because the arrival timing of spike trains on dendrites is responsible for this application. Axons are connected to synaptic capacitors. Since the output of each soma is $\oplus$, synaptic capacitors connected to $\ominus$ represent an excitatory synapse, while capacitors connected to $\oplus$ act as an inhibitory one. Consequently, spike trains on axons produce "efferent" spike trains on dendrites. Note that spike trains on dendrites cannot propagate on axons through synapses because each axon is directly connected with a soma that prohibits spike transmission from the axon to dendrites.

Figure 8 illustrates signal flows of spike trains when $N = 3$. In this example, neuron S_1 accepts afferent spike trains first. It transmits them to all dendrites through synaptic capacitors, which generates efferent spike trains on the dendrites. Subsequent afferent spike trains are annihilated by these efferent spike trains, which results in the inhibition of neurons. This phenomenon ("first come, first served" or "early arrival matters") represents temporal-domain neural competition. Again note that the term "inhibition" used here is not the conventional meaning of inhibition. Actually, it is "excitation" to produce efferent spike trains that annihilate afferent-input spike trains.

4. Simulation Results

We simulated the proposed circuits with $N = 3$ using a modified Monte Carlo method [4]. In the simulations, the supply voltage ($V_{\rm dd}$), bias voltage ($V_{\rm L}$), resistance (R), capacitance (C_i), and conductance of a tunnel junction were set at 4.4 mV, 2.4 mV, 440 MΩ, 10 aF, and 4 μS, respectively. The coupling and buffering capacitances were set at 2 aF. Each neuron receives periodic spikes from afferent inputs. The inter-spike interval was set at 30 ns. The time-lag between each afferent input was set at 3 ns, and node "A" accepted the first spike. Figure 9 plots the time courses for node voltages at the input nodes ("A", "B", and "C" in Fig. 7) and somas ("D", "E", and "F" in Fig. 7) when the temperature was set at 0 K. As expected, only one neuron "D" that received the first afferent input produced output spikes and resting neurons "E" and "F" did not produce output spikes, which indicates that competition in the time domain was successfully achieved by having inputs that carried encoding in the form of spike timing.

Our next interest is thermal-noise tolerance in the single-electron neural network. Table 1 shows the accuracy (success rate) dependence of neural competition on the network's temperature and $V_{\rm dd}$. The rate was calculated using the ratio of the number of spikes that arrived at the winning

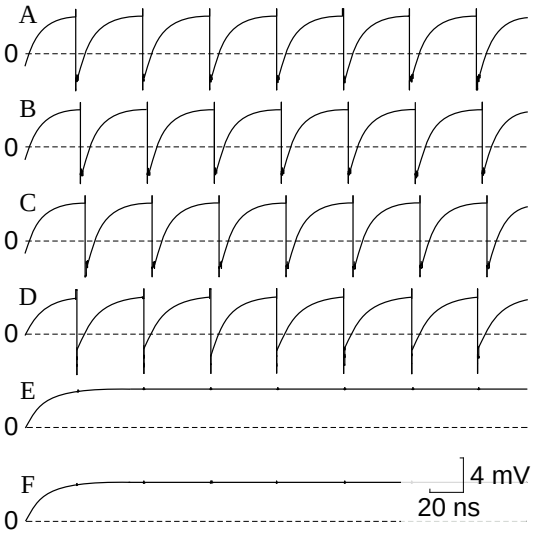

Figure 9 Time course for input (A-C) and output (D-F) nodes.

Temp \ $V_{\rm dd}$	3.8 mV	4 mV	4.2 mV	4.4 mV
0 K	0.04	0.88	0.96	1
0.01 K	0	0.79	1	1
0.1 K	0.01	0.79	1	1
1 K	0.21	0.38	0.08	0.2

Table 1 Calculated accuracy (success rate) for variable temperature and $V_{\rm dd}$.

neuron to that of afferent spikes (25 afferent spikes during 750 ns). We averaged three sets of simulation results with different random seeds. When the temperature was lower than 0.1 K and $V_{\rm dd} = 4.4$ mV, the circuit exhibited perfect neural competition. As $V_{\rm dd}$ decreased, the rate decreases as well because low $V_{\rm dd}$ prevents spike trains on dendrites.

5. Discussion

We designed a single-electron neuron circuit, aiming at exploring robust and fault-tolerant circuit architectures for nano-devices. We observed expected neural competition at quite a low temperature (≤ 1 K). A possible solution to further increase the operation temperature is to leave several winners (not one) to represent a winning "cluster" [3]. Although a large number of neurons are required, it will be an appropriate method of constructing fault-tolerant nanoelectronics systems.

Single-electron memory devices that store synaptic weights are necessary for constructing practical neural devices. To store the weights, we are trying to use a real-time memory on excitable fields where action potentials propagate on a circular excitable field and the direction of waves represents binary values [5].

The primary element in our circuit is a single-electron

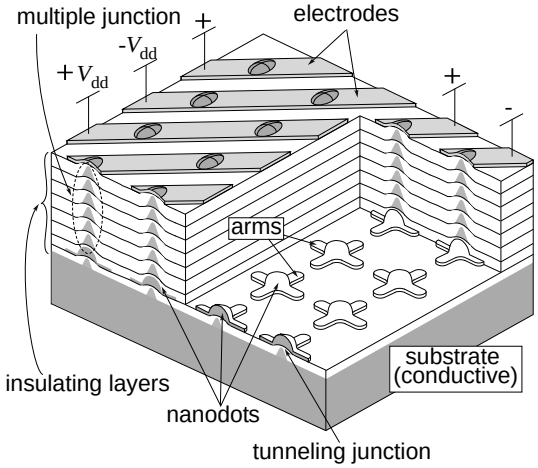

Figure 10 Possible structure of single-electron neural device.

oscillator coupled with several neighbors. The multiple-tunneling-junction oscillator is preferable for this element because it can be made without high resistance, which is difficult to implement on an LSI chip. Figure 10 shows possible three-dimensional and cross-sectional schematics for the possible structure of the device. Each oscillator consists of a conductive nanodot with four coupling arms, and there is a tunneling junction between the nanodot and the conductive substrate beneath it. Many series-connected junctions run between the nanodot and a positive-bias or a negative-bias electrode. Capacitive coupling between neighboring oscillators can be achieved by laying their coupling arms close to each other.

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