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On the modeling of log-domain LC ladder circuits

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Abstract–Log-domain filters are an intriguing form of current-mode circuits. They are universally regarded as externally-linear internally-nonlinear circuits in which each bipolar junction transistor operates in the forward-active mode at all times and acts as a static exponential non-linearity relating the collector current to the base-emitter voltage. This paper establishes sufficient conditions for the external linearity of single-ended and differential log-domain LC ladder circuits. However, differential log-domain LC ladder floating-capacitor circuits exhibit externally-nonlinear behaviour. Modeling the transistors as static non-linearities, the equations of these circuits are unable to describe their nonlinear behaviour. Simulations show the strong influence of parasitics on these dynamics.

1. Introduction.

Ideally log-domain filters [1] are current-mode circuits employing bipolar junction transistors (BJTs) whose operation is in the forward-active mode at all times and is not affected by the presence of parasitics. The BJT large-signal static exponential relationship between the collector current and the base-emitter voltage in the forward-active mode is first used to map input currents to the logarithmic form. Then analog processing is performed on the resulting log-domain voltages. At the end of the filtering process, the log-domain output voltages are converted back to the current domain using the BJT static exponential non-linearity once again. Due to the compression and expansion operations, log-domain filters are not particularly sensitive to noise, show low levels of distortion, exhibit high dynamic range and can be designed to satisfy the ever more demanding today's low-power and high-speed requirements.

Ideally the input-output behaviour of log-domain filters is linear. However, the internal non-linearity of such circuits is sometimes responsible for the occurrence of externally-nonlinear behaviour.

One of the most efficient log-domain circuit design techniques is the method of operational simulation of LC ladders [1]. This paper derives sufficient conditions for the externally-linear behaviour of single-ended and differential log-domain LC ladder circuits.

It is common practice to reduce the integrated circuit (IC) area of internally-linear fully-differential capacitively loaded circuits by replacing each pair of equal-value shunt capacitors connected between two nodes and ground with a single half-sized floating capacitor connected between these nodes. However, when such technique is applied to differential log-domain LC ladder circuits external linearity is lost [2]. The differential equations of these floating-capacitor circuits, derived under the common assumption that BJTs act as static exponential non-linearities, fail to describe the nonlinear behaviour under study. Simulations show that BJT internal parasitics play a significant role in these dynamics. Therefore, any reasonable model of these circuits must regard BJTs as dynamic non-linearities.

2. Simulation results for a log-domain LC ladder third-order Chebyshev low-pass filter.

The log-domain circuit design method of operational simulation of LC ladders [1] starts off from a LC ladder passive prototype meeting the desired specifications (Fig. 1a in the case of a third-order Chebyshev low-pass filter, where $r_1 = r_2 = 1\Omega$, $c_1 = c_3 = 0.1$ ∝F and $l_2 = 0.05$ ∝H for a maximum pass-band ripple width of 1 dB and a cut-off frequency of 3 MHz). Then application of Kirchhoff's current and voltage laws (KCL and KVL respectively) allows to derive the expressions for the voltages across the capacitors and the currents through the inductors of the prototype. These expressions are represented by a signal flow graph (SFG), as in Fig. 1b for the case under study. Inserting in the SFG expansion stages before each summer and at the output and compression blocks after any integrator and at the input, a log-domain SFG is obtained (Fig. 1c in this example). The *EXP* and *LOG* functions, implemented respectively by expansion and compression stages, are one the inverse of the other and are defined by

$$y = EXP(x) = I_o \exp(0.5x/V_T) - I_o \quad EXP: R. \quad S = \{y. \ R: y > -I_o\}$$

$$x = LOG(y) = 2V_T \ln[(I_o + y)/I_o] \quad LOG: S. \quad R \quad (1)$$

This pair of complementary functions makes possible to obtain the transistor-level realization of the log-domain LC ladder filter (Fig. 2a for this case, where the above specifications for the passive prototype of Fig. 1a are met if $I_o = 100$ μA, C_1=$C_3 = 0.2$ nF and $C_2 = 0.1$ nF) through the use of positive (eg. Q_5-Q_8 in Fig. 2a) and negative (eg. Q_9-Q_{12} in Fig. 2a) log-domain cells. In fact, application of the Translinear Principle [1] makes clear that, at least ideally, the current sourced to (sunk from) a grounded capacitor by a positive (negative) log-domain cell is exponentially related to the difference between the input

and output voltages of the cell.

Unlike its passive prototype, the log-domain circuit has neither resistors nor inductors and employs much smaller capacitors, thus being suitable for IC realization.

Most non-idealities experienced by the IC, such as fluctuation of circuit parameters with temperature, may be canceled out using a differential version. Fig. 2b shows the log-domain LC ladder basic integrator. Its differential counterpart is obtained cross-coupling the inputs of two identical integrators with capacitors two times larger than in the single-ended case (Fig. 2c). This procedure can be applied a number of times to derive the differential version of the log-domain filter (Fig. 3 in this example, where capacitors are double the size and all other circuit elements are unchanged with respect to the single-ended filter satisfying the same design requirements given above).

Futhermore, in order to save area on the IC, each pair of equal-value shunt capacitors, connected between two nodes and ground, is generally replaced with a single half-sized floating capacitor connected between these nodes.

The simulation results, shown below, provide numerical evidence for the theorems of sections 3 and 4. The supply voltages are set to ±1.5 V and the devices modeling the npn and pnp BJTs are perfectly matched with parameter values being those of the 2N3904 with the exception of the forward-current gain, set to the typical value of 100.

An extensive number of simulations show that the differential shunt-capacitor circuit of Fig. 3 does not exhibit nonlinear dynamical behaviour but rather behaves as expected of a log-domain filter: for example, if a sine wave with frequency 100 kHz and amplitude 10 ∝V (one tenth of the value of I_o) is inserted at the input of the LC ladder passive prototype of Fig. 1a with initial conditions set to 0, the corresponding dynamical behaviour is identical to that of the circuit of Fig. 3 with same forcing and initial conditions (Fig. 4). Moreover, as expected, in the latter case BJTs operate in the forward-active mode at all times and each log-domain cell acts as a static exponential non-linearity (Fig. 5, left). Setting to zero the diffusion and junction capacitances in the PSpice model of each BJT does not affect these simulation results, in agreement with the common practice to neglect them for modeling purposes.

On the other hand, behaviour of the floating-capacitor version of the circuit of Fig. 3 is not externally-linear. Even in the autonomous case, perturbation of this circuit from the equilibrium gives rise to a rich nonlinear dynamical behaviour as bifurcation parameter C_1 is adjusted in small steps [2]. The theoretical results concerning the operation of log-domain circuits fail for this circuit: each BJT does not necessarily operate in the forward-active mode at all times and log-domain cells do not act anymore as static exponential non-linearities (Fig. 5, right, where $C_1 = 0.585$ nF and chaos is observed). When parasitics are removed from the model of each BJT, PSpice fails to complete the run of simulations. Since the nonlinear behaviour of this circuit depends strongly on the dynamics of the BJT small internal capacitances, it is vital

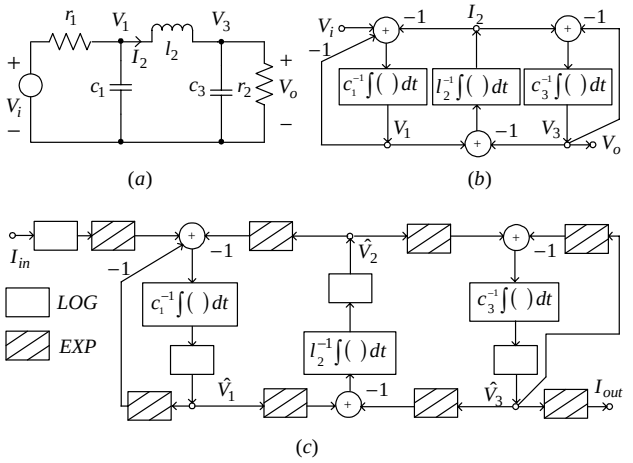

Fig. 1 LC ladder prototype (a), linear SFG (b) and log-domain SFG (c) of a third-order Chebyshev low-pass filter.

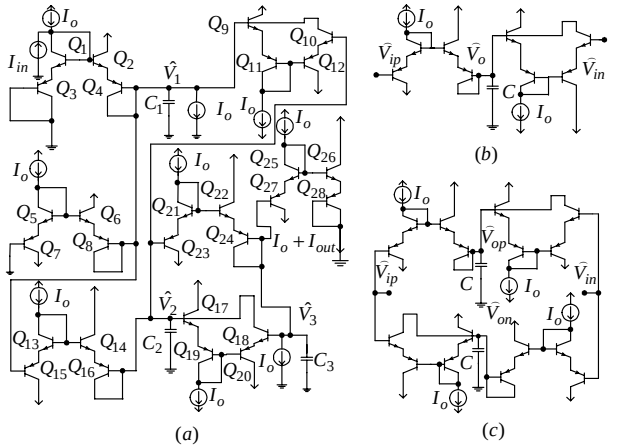

Fig. 2 Log-domain LC ladder implementations of a third-order Chebyshev low-pass filter (a), a basic integrator (b) and a differential integrator (c).

to take account of them for modeling purposes.

3. External linearity of log-domain LC ladder circuits.

Throughout the paper each log-domain LC ladder cell is modeled as a static exponential non-linearity. Let the n state variables of the linear, time-invariant single-input system corresponding to a n[th]-order LC ladder passive prototype be the voltages across the capacitors and the currents through the inductors. As explained in section 2, the time derivatives of these state variables can be obtained by applying KCL and KVL to the passive filter:

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{b}u \qquad (2)$$

where $\mathbf{x}$. R^n is a nx1 state vector, $\mathbf{A}$ is a nxn strictly Hurwitz matrix, $\mathbf{b}$ is a nx1 input vector and u is a scalar input. For example, eq. (2) models the dynamic behaviour of the passive prototype of Fig. 1a for n = 3, $u = V_i$ and

$$\mathbf{x} = \begin{pmatrix} V_1 \\ I_2 \\ V_3 \end{pmatrix} \mathbf{A} = \begin{pmatrix} -1/c_1 & -1/c_1 & 0 \\ 1/l_2 & 0 & -1/l_2 \\ 0 & 1/c_3 & -1/c_3 \end{pmatrix} \mathbf{b} = \begin{pmatrix} 1/c_1 \\ 0 \\ 0 \end{pmatrix} \qquad (3)$$

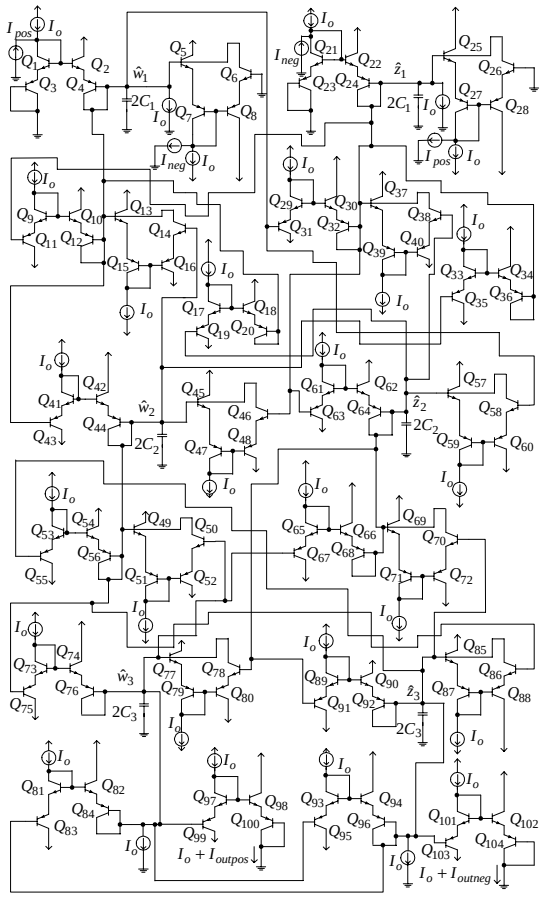

Fig. 3 Differential version of the circuit of Fig. 2a.

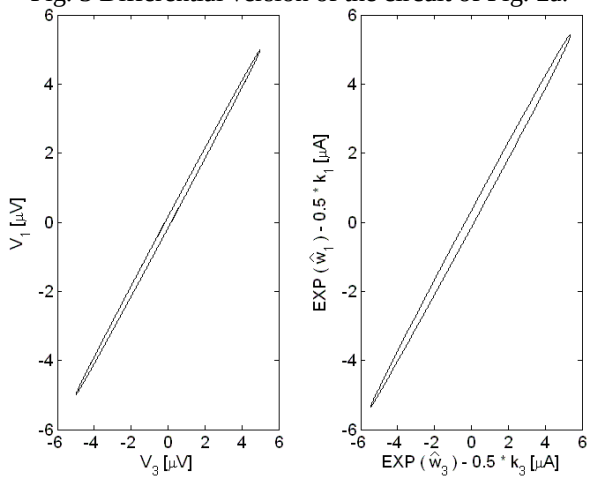

Fig. 4 State-plane projections of the elliptical attractors of the sinusoidally-driven systems corresponding to the prototype of Fig. 1a (left) and to the circuit of Fig. 3 (right, where k_1 = 78.5 ∝A and k_3 = 240 ∝A).

The design technique, outlined in section 2, yields the following state-space equations for the n[th]-order system corresponding to the single-ended log-domain circuit:

$$\dot{\mathbf{V}} = \mathbf{A}\mathbf{V} + \mathbf{b}u_s \qquad (4)$$

where $\mathbf{V}^T = [EXP(\hat{V}_1) \quad \cdots \quad EXP(\hat{V}_n)]$. S^n, u_s is the input current and $\hat{V}_i$ is the voltage across grounded capacitor C_i

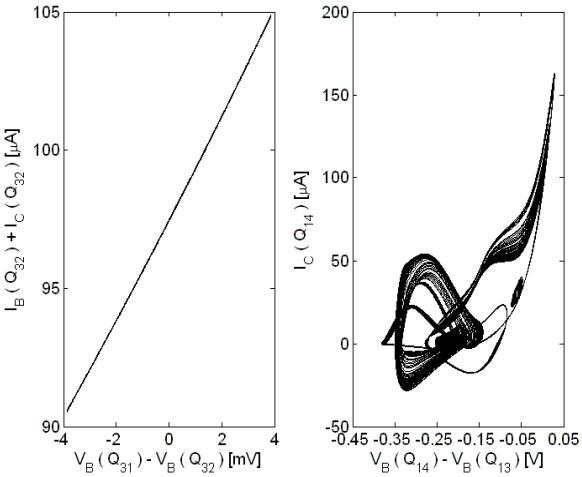

Fig. 5 Left: Static exponential non-linearity introduced by positive cell Q_{29}-Q_{32} in the circuit of Fig. 3 with sinusoidal forcing. Right: Dynamic behaviour of negative cell Q_{13}-Q_{16} in the floating-capacitor version of the circuit of Fig. 3 with neither input nor output cells (C_1 = 0.585 nF).

with $i \in I_n = \{1, 2, \ldots, n\}$. As an example, the dynamics of the circuit of Fig. 2a are described by eq. (4) with n = 3, **A** and **b** given in (3) and $u_s = I_{in}$.

The synthesis technique of section 2 yields the following state-space equations for the (2n)[th]-order systems corresponding to the differential log-domain filters:

$$\begin{pmatrix} \dot{\mathbf{W}} \\ \dot{\mathbf{Z}} \end{pmatrix} = \frac{1}{2}\begin{pmatrix} \mathbf{A} & -\mathbf{A} \\ -\mathbf{A} & \mathbf{A} \end{pmatrix}\begin{pmatrix} \mathbf{W} \\ \mathbf{Z} \end{pmatrix} + \begin{pmatrix} \mathbf{b} \\ -\mathbf{b} \end{pmatrix} u_d \qquad (5)$$

where $\mathbf{W}^T = [EXP(\hat{w}_1) \quad \cdots \quad EXP(\hat{w}_n)]$. S^n, $u_d = 0.5(u_+ - u_-)$, u_+ and u_- are the positive and negative input currents respectively and $\mathbf{Z}^T = [EXP(\hat{z}_1) \quad \cdots \quad EXP(\hat{z}_n)]$. S^n. Finally $\hat{w}_i$ and $\hat{z}_i$ are the voltages across two grounded shunt capacitors of value C_i. For instance, the dynamic behaviour of the circuit of Fig. 3 is described by eq. (5) with n = 3, **A** and **b** given in (3), $u_+ = I_{pos}$ and $u_- = I_{neg}$.

Eq. (5) disguises a relationship between each pair of state variables $(\hat{w}_i, \hat{z}_i)$: $EXP(\hat{z}_i) = -EXP(\hat{w}_i) + k_i$, where k_i is a constant larger than $-2I_o$. Using this and then setting $\xi_i = EXP(\hat{w}_i) - 0.5k_i$, the (2n)[th]-order system (5) is forced by the circuit topology to behave as the following n[th]-order system:

$$\dot{\boldsymbol{\xi}} = \mathbf{A}\boldsymbol{\xi} + \mathbf{b}u_d \qquad (6)$$

where $\boldsymbol{\xi}^T = (\xi_1 \quad \cdots \quad \xi_n)$. $(S - 0.5k_1) \cdot \ldots \cdot (S - 0.5k_n)$.

Eqs. (2), (4) and (6), modeling the original passive prototypes, the single-ended and the differential log-domain LC ladder filters respectively, have different ranges of validity: $\mathbf{x}$. R^n for (2), $\mathbf{V}$. S^n for (4) and $\boldsymbol{\xi}$. $(S - 0.5k_1) \cdot \ldots \cdot (S - 0.5k_n)$ for (6). However, letting $u = u_s = u_d$, if it is ensured that $\mathbf{x}$. S^n at all instants of time, then $\mathbf{x}$ is the same as $\mathbf{V}$, systems (2) and (4) are

identical and solutions of (2) are also solutions of (4). Also, ensuring that $\mathbf{x}$. $(S-0.5k_1)\cdot \ldots \cdot (S-0.5k_n)$ for any $t \geq 0$, $\mathbf{x}$ is equivalent to ξ, system (2) is the same as (6) and trajectories of (2) are trajectories of (6) as well.

If at any instant of time $\|\mathbf{x}(t)\|_\infty \leq \sigma I_o$, where $0 < \sigma < 1$ and I_o= min (I_o, I_o +0.5k_1, …, I_o +0.5k_n), then (2), (4) and (6) are identical one another and, as a result, log-domain circuits cannot observe nonlinear dynamical behaviour. Sufficient conditions for this to occur are derived next.

Theorem: Given a strictly Hurwitz matrix **A**, it is always possible to choose sufficiently small initial conditions and input amplitude of (2) such that $\|\mathbf{x}(t)\|_\infty \leq \sigma I_o$ for any $t \geq 0$, where $0 < \sigma < 1$ and I_o= min (I_o, I_o +0.5k_1, …, I_o +0.5k_n).

Proof: Given $\mathbf{x}(t) \in R^n \; \forall t \geq 0$, let

$$\|\mathbf{x}\| = \sup_{t=0} \|\mathbf{x}(t)\|_\infty \quad \text{and} \quad \|u\| = \sup_{t=0} |u(t)|$$

Since **A** is a strictly Hurwitz matrix, there exist two constants $\alpha \geq 0$ and $\beta \geq 0$ such that

$$\|\mathbf{x}\| \leq \alpha \|\mathbf{x}(t=0)\|_\infty + \beta \|u\|$$

This implies: $\|\mathbf{x}\| \leq \sigma I_o$ if $\alpha \|\mathbf{x}(t=0)\|_\infty + \beta \|u\| \leq \sigma I_o$ Δ

4. Inappropriateness of the BJT static model for differential LC ladder floating-capacitor circuits.

For the floating- capacitor circuits with BJTs modeled as static exponential non-linearities, eqs. (1) and (5) yield:

$$\begin{pmatrix} \dot{\mathbf{w}} - \dot{\mathbf{z}} \\ \dot{\mathbf{z}} - \dot{\mathbf{w}} \end{pmatrix} = \frac{2V_T}{I_o} \begin{pmatrix} \mathbf{D}_{\hat{\mathbf{w}}}\mathbf{A} & -\mathbf{D}_{\hat{\mathbf{w}}}\mathbf{A} \\ -\mathbf{D}_{\hat{\mathbf{z}}}\mathbf{A} & \mathbf{D}_{\hat{\mathbf{z}}}\mathbf{A} \end{pmatrix} \begin{pmatrix} \mathbf{W} \\ \mathbf{Z} \end{pmatrix} + \frac{4V_T}{I_o} \begin{pmatrix} \mathbf{D}_{\hat{\mathbf{w}}}\mathbf{b} \\ -\mathbf{D}_{\hat{\mathbf{z}}}\mathbf{b} \end{pmatrix} u_d \quad (7)$$

with $\mathbf{D}_{\hat{\mathbf{w}}} = diag\{\exp(-0.5\hat{w}_i/V_T)\}$, $\mathbf{D}_{\hat{\mathbf{z}}} = diag\{\exp(-0.5\hat{z}_i/V_T)\}$

$\mathbf{w}^T = [\hat{w}_1 \quad \cdots \quad \hat{w}_n]$ and $\mathbf{z}^T = [\hat{z}_1 \quad \cdots \quad \hat{z}_n]$.

For instance, the dynamic behaviour of the floating-capacitor version of the circuit of Fig. 3 is described by eq. (7) with $u_+ = I_{pos}$, $u_- = I_{neg}$, n = 3 and **A** and **b** given in (3). For $u_d = 0$, at any instant of time (7) yields:

$$(\mathbf{D}_{\hat{\mathbf{w}}} - \mathbf{D}_{\hat{\mathbf{z}}})\mathbf{A}\mathbf{W} = (\mathbf{D}_{\hat{\mathbf{w}}} - \mathbf{D}_{\hat{\mathbf{z}}})\mathbf{A}\mathbf{Z} \quad (8)$$

In the autonomous case solutions to eq. (7) are not compatible with the nonlinear behaviour exhibited by the floating-capacitor circuits with zero inputs, as proved next.

Theorem: For a strictly Hurwitz matrix **A**, in the autonomous case eq. (7) has only two possible solutions:

a) $\hat{w}_i = \hat{z}_i \; \forall i$ and $\forall t \geq 0$

b) $\hat{w}_i = 8$ or $\hat{z}_i = 8$ for some i and $\forall t \geq 0$

Proof: Let a_i^T be the i^{th} row of **A** and define

$$\mathbf{D}_{\hat{\mathbf{w}}} - \mathbf{D}_{\hat{\mathbf{z}}} = diag\{d_i\} \quad \text{and} \quad \boldsymbol{\rho} = \{EXP(\hat{w}_i) - EXP(\hat{z}_i)\} = \{\cdot_i\}$$

1. Assume $\hat{w}_i \neq \hat{z}_i \; \forall i$ and some t ≥ 0. Since $\mathbf{D}_{\hat{\mathbf{w}}} - \mathbf{D}_{\hat{\mathbf{z}}}$ and **A** are non-singular, from (8) $\hat{w}_i = \hat{z}_i \; \forall i$, i.e. a contradiction.

2. Assume $\hat{w}_i = \hat{z}_i \; \forall i$ and $\forall$t ≥ 0. This is a possible finite solution to eq. (7) in the autonomous case (case a).

3. Let $I_r = \{i_1, i_2, \ldots, i_r\} \subset I_n$ with $i_1 < i_2 < \ldots < i_r$.

Assume $\hat{w}_i \neq \hat{z}_i \; \forall i \in I_r$ and $\hat{w}_i = \hat{z}_i \; \forall i \in I_r^C$ for some $t \geq 0$.

Since d_i . 0 $\forall i \in I_r$ and $d_i = 0 \; \forall i \in I_r^C$, (8) becomes $\mathbf{D}_{\mathbf{II}}\left(a_{i_1}^T \quad \cdots \quad a_{i_r}^T\right)^T \boldsymbol{\rho} = \mathbf{0}$ where $\mathbf{D}_{\mathbf{II}} = diag\{d_i\} \; \forall i \in I_r$.

Since $\mathbf{D}_{\mathbf{II}}$ is non-singular, ρ_i . 0 . $i \in I_r$ and $\rho_i = 0$. $i \in I_r^C$, this yields:

$$\mathbf{A}_{\mathbf{II}}\left(\cdot_{i_1} \quad \cdots \quad \cdot_{i_r}\right)^T = \mathbf{0} \quad (9)$$

where $\mathbf{A}_{\mathbf{II}}$ is the submatrix of **A** obtained by retaining the rows and columns with indeces $i \in I_r$. If $\mathbf{A}_{\mathbf{II}}$ were non-singular, this would imply $\rho_i = 0$. $i \in I_r$, i.e. a contradiction. So $\mathbf{A}_{\mathbf{II}}$ must be singular. In this case, letting $u_d = 0$, the first n rows of (7), except those corresponding to indeces $i \in I_r$, yield:

$$\mathbf{D}_{\hat{\mathbf{w}}\mathbf{I}^c\mathbf{I}^c}\mathbf{A}_{\mathbf{I}^c\mathbf{I}}\left(\cdot_{i_1} \quad \cdots \quad \cdot_{i_r}\right)^T = \mathbf{0} \quad (10)$$

where $\mathbf{D}_{\hat{\mathbf{w}}\mathbf{I}^c\mathbf{I}^c}$ is the submatrix of $\mathbf{D}_{\hat{\mathbf{w}}}$ formed through elimination of rows and columns with indeces $i \in I_r$ and $\mathbf{A}_{\mathbf{I}^c\mathbf{I}}$ is the submatrix of **A** obtained by removing rows and retaining columns with indeces $i \in I_r$. Eq. (10) is satisfied by unbounded solutions (case b), but if it is assumed that $\hat{w}_i$ and $\hat{z}_i$ are finite $\forall i \in I_n \; \forall t \geq 0$, then eq. (10) yields:

$$\mathbf{A}_{\mathbf{I}^c\mathbf{I}}\left(\cdot_{i_1} \quad \cdots \quad \cdot_{i_r}\right)^T = \mathbf{0} \quad (11)$$

Combination between (9) and (11) gives $\mathbf{A}\boldsymbol{\rho} = \mathbf{0}$. If this were true, **A** would have an eigenvector with eigenvalue equal to 0, i.e. a contradiction since **A** is Hurwitz. Δ

Thus, using the BJT static model, the equation of the floating-capacitor circuits, i.e. (7), in the autonomous case provides two possible solutions: either the voltage across each capacitor is zero $\forall t \geq 0$ or some nodal voltage assume an infinite value. Both solutions are unacceptable in any real circuit. In any event, eq. (7) fails to model the rich dynamics of the floating-capacitor circuits. As suggested by simulation results of section 2, BJT parasitic effects must be taken into account for modeling purposes.

Conclusions

Log-domain filters are generally regarded as externally-linear circuits in which operation of BJTs is essentially unaffected by its internal capacitances. Sufficient conditions for the external linearity of log-domain LC ladder circuits are derived. However, log-domain circuit theory is not able to describe the nonlinear behaviour exhibited by the differential LC ladder floating-capacitor circuits, since neglects the dynamics of the BJT parasitics.

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