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An Algorithm for the "Effective Capacitance" of CMOS Gate with Interconnect Load

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Abstract — In this paper, we propose an algorithm for computing the effective capacitance of CMOS gate with interconnect load in deep submicron technology. Compared with previous methods, the new approach is accurate and does not require pre-simulation table. The experimental results show that it is in agreement with Spice simulation.

1. Introduction

With the rapid progress of Integrated Circuit process technology, interconnect wire has become an important factor that influences the performance of chip. In deep submicron technology, interconnect wire delay takes the largest portion of the whole chip delay. Currently, the interconnect resistance is equal or larger than the gate resistance and part of the load capacitance is shielded "seen" from the gate. The RC-π load model [1] is used to model a general RC tree because it is found to be accurate sufficiently when compared with actual circuit.

However, the empirical gate-delay equations have only one pure capacitive load C_L, and the RC-π model has three parameters C_1, C_2 and R. Therefore, it is difficult to calculate the gate-delay with RC-π model. In order to maintain compatibility with the empirical gate-delay model, the effective capacitance C_{eff} of interconnect load was proposed, which accounts for the reduction in the gate delay due to the shielding component [2].

A number of research papers [3]-[6] have been published on calculating the effective capacitance of interconnect wire. In [4] and [6], the effective capacitance is obtained based on the table of a pre-simulation result. However, these methods need pre-simulation with large storage resource. In [3] and [5], the authors obtain the capacitance value by replacing the driver gate with a resistance in theoretical model. However, the driving resistance in their model is determined by the output load and input transition time. There is a great variation in the above mentioned parameters and therefore one can not obtain an accurate result.

This paper describes a new algorithm to compute the effective capacitance for interconnect load. The new algorithm is based on the analytical expressions stated in this paper and is considerably accurate without requiring pre-simulation table. The experimental results show it is close to the Spice simulation.

The rest of this paper is organized as follows. Section 2 gives a detailed description of the proposed algorithm to compute the effective capacitance. Results for a 0.25-um CMOS process are presented in Section 3. Finally, conclusions are made in Section 4.

2. Proposed algorithm

2.1. The definition of effective capacitance

Figure 1 shows the gate driving an RC-π load and capacitance C_{eff} load. The effective capacitance C_{eff} is defined to be a single capacitance that will results in the same 50% point delay as the RC-π model [2]. Then, the value of C_{eff} is determined by equating the charges transferred to C_{eff} and to the actual RC-π load over the interval, namely between $t = 0$ and $t = t_D$ [4],

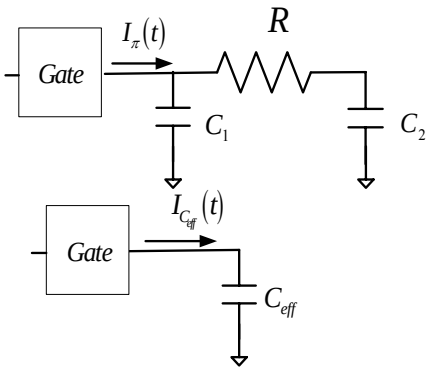

Fig.1. The gate driving an RC-π load and effective capacitance C_{eff}.

where t_D is the time of the output voltage from initial

point to 50% point. Therefore, we have

$$\frac{1}{t_D}\int_0^{t_D} I_\pi(t)\,dt = \frac{1}{t_D}\int_0^{t_D} I_{C_{eff}}(t)dt\,, \qquad (1)$$

where $I_\pi(t)$ is the current flowing into the RC- π load in Fig.1, and $I_{Ceff}(t)$ is the current flowing into the effective capacitance C_{eff}. Moreover, the LHS of Eq.(1) is the average current flowing into RC-π load over the time zero to t_D, and the RHS is that of C_{eff}.

2.2. Analytical Expressions

The charge Q from the gate with an average current $\bar{I}$ flowing into the load over an interval t is given by $Q = \bar{I}t$. Therefore, the charge RC- π load Q_π now equals the charge the effective capacitance Q_{Ceff} as indicated in Fig.1.

$$Q_\pi = Q_{Ceff}\,. \qquad (2)$$

Figure 2 shows that how the effective capacitance is obtained from RC-π load. In the figure, we assume the initial charges of all the capacitances are zero. From Fig.2 it can be inferred that $C_{eff} = C_1 + C_{eff}'$. Therefore, we have

$$Q_{Ceff} = Q_{C1} + Q_{Ceff'}\,, \qquad (3)$$

where Q_{C1} is the charge of capacitance C_1, $Q_{Ceff'}$ is the charge of the capacitance C_{eff}'. This idea can be extended for the RC-π load. Therefore, we obtain that

$$Q_\pi = Q_{C1} + Q_{C2}\,, \qquad (4)$$

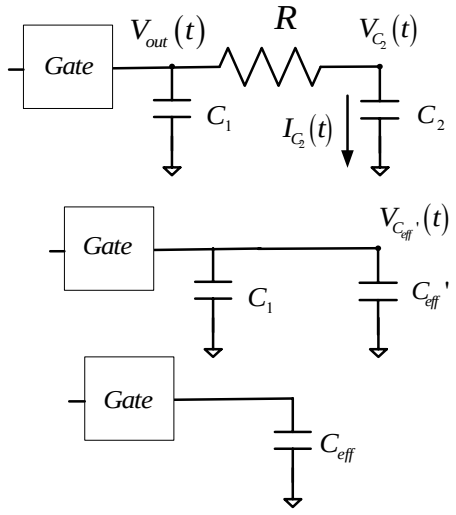

Fig.2. Effective capacitance is obtained from RC-π load.

where Q_{C1} is the charge of capacitance C_1, Q_{C2} is the charge of the capacitance C_2.

Substituting Eqs. (3) and (4) into (2), we have

$$Q_{C2} = Q_{Ceff'}\,, \qquad (5)$$

From the relation $Q = CV$, where V is the voltage of capacitance C and Q is the charge of capacitance C, Eq.(5) becomes

$$C_2 V_{C2}(t) = C_{eff}'\,V_{Ceff'}(t)\,, \qquad (6)$$

where $V_{C2}(t)$ is the voltage of capacitance C_2, $V_{Ceff'}(t)$ is the voltage of capacitance C_{eff}'. When $t = t_D$, $V_{Ceff'}(t)$ equals $V_{out}(t)$. Therefore, C_{eff}' can be written as follow [4]:

$$C_{eff}' = \frac{C_2 V_{C2}(t)}{V_{out}(t)}\Big|_{t=t_D}\,. \qquad (7)$$

Applying KVL to RC-π load circuit in Fig.2, we obtain

$$RI_{C2}(t) + V_{C2}(t) = V_{out}(t)\,. \qquad (8)$$

The current flowing into capacitance C_2 is

$$I_{C2}(t) = C_2\frac{dV_{out}(t)}{dt}\,. \qquad (9)$$

Using Eq.(9) , Eq.(8) becomes

$$RC_2\frac{dV_{C2}(t)}{dt} + V_{C2}(t) = V_{out}(t)\,. \qquad (10)$$

From Eq.(10), $V_{C2}(t)$ is expressed as

$$V_{C2}(t) = e^{-\frac{t}{RC_2}}\left[\frac{1}{RC_2}\int_o^t V_{out}(t)\,e^{\frac{t}{RC_2}}dt + k\right], \qquad (11)$$

where k is a constant. The condition $k = 0$ is determined by $V_{C2}(t)|_{t=0} = 0$. If $V_{out}(t)$ is known then we can get $V_{C2}(t)$, and C_{eff}' can be obtained with Eq.(7).

2.3. Output Waveform

It is well known that the output waveform of the gate $V_{out}(t)$ changes linearly around the 50% point of the output waveform [7][8][9]. CMOS gates can be modeled using a combination of quadratic and linear functions that correspond to the operating regions of the MOSFET's [10]. Therefore, the output waveform of CMOS gate can be assumed as follows [2]:

$$V_{out}(t)=\begin{cases} V_{initial}-ct^2 & 0\le t\le t_x \\ a+b(t-t_x) & t_x\le t\le t_D \end{cases}. \quad (12)$$

Staring at the initial voltage $V_{initial}$, the waveform is quadratic to the 20% point t_x. In Eq.(12), $V_{initial}$ is equal to V_{DD} for a falling waveform, and equal to zero for rising waveform. From the 20% point to the midpoint, the transistors are in the active region. Therefore, the waveform is assumed to be linear up to 50% point t_D. Moreover, a, b and c are the constants, a is equal to $0.2\,V_{DD}$ for rising waveform and $0.8\,V_{DD}$ for falling waveform. The function of output voltage $V_{out}(t)$ is continuous at $t=t_x$. Therefore,

$$b=\frac{0.3V_{DD}}{t_D-t_x} \quad (13)$$

and

$$c=\frac{b}{-2t_x}. \quad (14)$$

The values of t_x and t_D can be determined by using a gate pre-characterization from the output waveform, and expressed as follows [9]:

$$t_D=f\left(t_{in},C_L\right) \quad (15)$$

and

$$t_x=g\left(t_{in},C_L\right), \quad (16)$$

where t_{in} is the input signal transition time from zero to 100% of its steady-state value.

2.4. Algorithm for Calculating Effective Capacitance

Using Eqs.(11) and (12), $V_{C2}(t)$ now becomes

$$V_{C2}(t)|_{t=t_D}=\frac{V_{DD}}{2}-\frac{3V_{DD}}{10}\frac{RC_2}{t_D-t_x}+\frac{3}{10}\frac{V_{DD}(RC_2)^2}{t_x(t_D-t_x)}e^{-\frac{t_D-t_x}{RC_2}}\left(1-e^{-\frac{t_x}{RC_2}}\right). \quad (17)$$

Since the output voltage is $V_{out}(t)|_{t=t_D}=V_{DD}/2$, we obtain the expression of effective capacitance as follow:

$$C_{eff}=C_1+C_2\left(1-\frac{3}{5}\frac{RC_2}{t_D-t_x}+\frac{3}{5}\frac{(RC_2)^2}{t_x(t_D-t_x)}e^{-\frac{t_D-t_x}{RC_2}}\left(1-e^{-\frac{t_x}{RC_2}}\right)\right). \quad (18)$$

From Eq.(18) we infer that C_{eff} is C_1+C_2 when the resistance is zero, and C_1 when the resistance R tends to infinity.

We use the following iterative procedure to compute the effective capacitance C_{eff}.

1. Set an initial value $C_{eff}=C_1+C_2$.
2. Obtain the time t_D and t_x using Eqs.(15), and (16) with effective capacitance C_{eff}.
3. Compute a new value of C_{eff} using the parameters t_D, t_x of step 2.
4. Set the above new value equal to C_{eff} and go back to step 2 until the iteration converges.

This procedure usually converges in three or four iterations. Then, the delay of gate can be obtained using the effective capacitance C_{eff}.

The effective capacitance C_{eff} in Eq. (18) is determined in above method. Note that the equation of C_{eff} in [2] is obtained by substituting Eq. (12) approximated gates output waveform into Eq. (1) directly with an additional approximation which may result in some errors. However, the equation of C_{eff} in this paper is obtained by substituting Eq.(12) into Eqs.(7) and (11) without additional approximation.

3. Experimental Results

All simulations in this paper are performed for a 0.25-um technology process. Figure 3 gives the comparison between the proposed algorithm and the Spice simulation when the resistance is varied from zero to $1000\,\Omega$. While performing the simulations the CMOS inverter transistor widths are $W_n/W_p=10\mu/21.4\mu$. Also the values of C_1 and C_2 in the RC-π circuit are $C_1=0.1pF/C_2=0.4\,pF$, and the input signal transition time $t_t=200\,ps$.

From Fig.3 we infer that when the resistance becomes larger, the effective capacitance decreases and most of the capacitance of interconnect wire is shielded. For most interconnect wires, the resistance should be much smaller than $1000\,\Omega$ (about $7mm$ length wires for 0.25-um process). Therefore, the proposed algorithm is accurate.

Figure 4 provides the comparison between the proposed algorithm and the Spice simulation when the gate widths are varied from $W_n/W_p=0.5\mu/1.07\mu$ to $W_n/W_p=25\mu/53.5\mu$. The ration of the PMOS width to the NMOS width W_p/W_n always remains at $2.14/1$. The values of C_1, C_2 R and R in the RC- π circuit are $C_1=0.1pF/C_2=0.4\,pF/R=300\Omega$, and the input signal transition time is $t_t=200\,ps$.

From Fig.4, it is inferred that when the width of gate increases, the effective capacitance decreases. The reason for the decrease in C_{eff} can be explained from the fact that the gate resistance decreases with increase in the width of transistor. The interconnect wire resistance now

is larger than the gate resistance. Therefore, more capacitance of gate load is shielded by the resistance of the interconnect wire. Therefore, the effective capacitance decreases. Figure 4 shows that the proposed algorithm is close to the Spice simulation result. Especially when the width of transistor is small, the results obtained by using the proposed algorithm have almost same values as the Spice simulation.

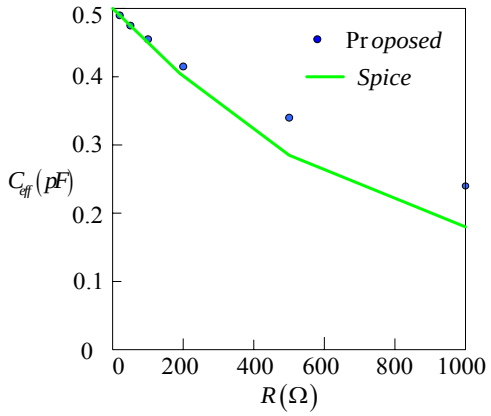

Fig.3. Comparison between the proposed algorithm and the Spice simulation when the resistance is varied.

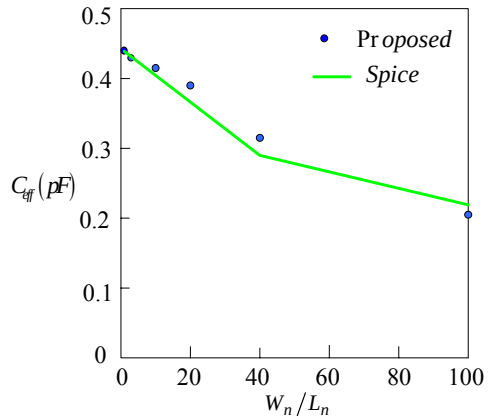

Fig.4. Comparison between the proposed algorithm and the Spice simulation when the gate width is varied.

4. Conclusions

This paper presents an efficient algorithm for calculating the effective capacitance of CMOS gate with interconnect load. Compared with the methods [5], the proposed method does not require pre-simulation table. In addition, the proposed method is more accurate than that [2]. The results of our proposed algorithm are in agreement with the Spice simulation.

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