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Low-Voltage, Low-Distortion and Rail-to-Rail CMOS Sample and Hold Circuit

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Abstract—In this paper, we propose a S/H circuit with the clock boost technique and the input signal tracking technique. The proposed circuit generates the clock with the amplitude of $VDD + v_{in}$, and the clock is used to control the MOS switch. By applying this circuit to a S/H circuit, we can deal with the rail-to-rail signal with maintainng low distortion. Furthermore, the hold error caused by the charge injection and the clock feedthrough can be also reduced by using the dummy switch. The Star-HSPICE simulation results are reported in this paper.

1. Introduction

The portable electronic market has accomplished explosive growth, and advance in CMOS technology has led designers towards low-voltage operation and mixed-signal systems. Therefore, a date converter operated under low-voltage will be an essential component of the portable electronic. Sample and hold (S/H) circuits are widely used in the discrete analog circuits and play an important role in the design of data converter. In analog switches used in the S/H circuits, rail-to-rail signal swing capability is required for maintaining high signal to noise ratio. However, it is difficult to realize it because of two issues. One is that the analog switches cannot be deeply turned on because enough overdrive voltage cannot be supplied to gates of MOS switches under the low-voltage condition. The other is that the output signal is distorted by the on-resistance, which is varied by the difference between input voltage of the MOS switch and the clock voltage. In order to overcome these issues, the clock boost technique [1],[2] and the input signal tracking technique attract [3],[4]. However, there is a problem that a hold error increases by the charge injection and clock feedthrough. This error becomes larger with using the boosted clock.

In this paper, a simple S/H circuit with the clock boost technique and the input signal tracking technique is proposed. The proposed circuit consists of two simple clock boosters with input tracking circuit and a dummy switch. As the results, the proposed circuit reduce the effect of charge injection and feedthrough with maintaining low-voltage, low-distortion and rail-to-rail operation. The proposed circuit is evaluated through Star-HSPICE simulation with the process parameters of CMOS 0.35μm. The results are shown in this paper.

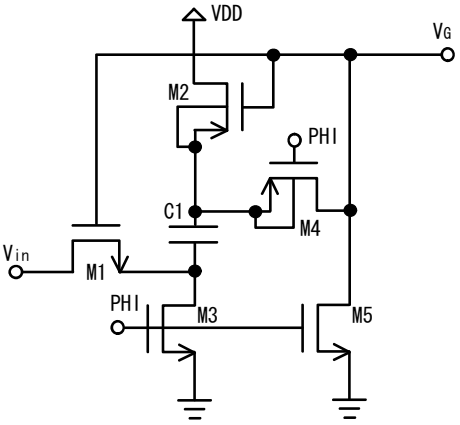

Figure 1: Clock generator with the boost and V_{in} tracking technique.

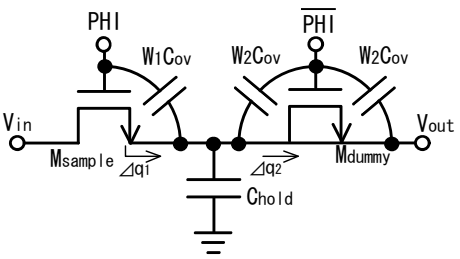

Figure 2: Dummy switch.

2. The proposed S/H Circuit

The clock generator with the boost and V_{in} tracking technique is shown in Fig. 1. The circuit is controlled by a clock *PHI* and operates as follows.

When *PHI* is high, *VDD* is applied across $C1$ since $M2$ and $M3$ are turned on. Simultaneously $M1$ and $M4$ are turned off, and $M5$ is turned on. V_G results in becoming

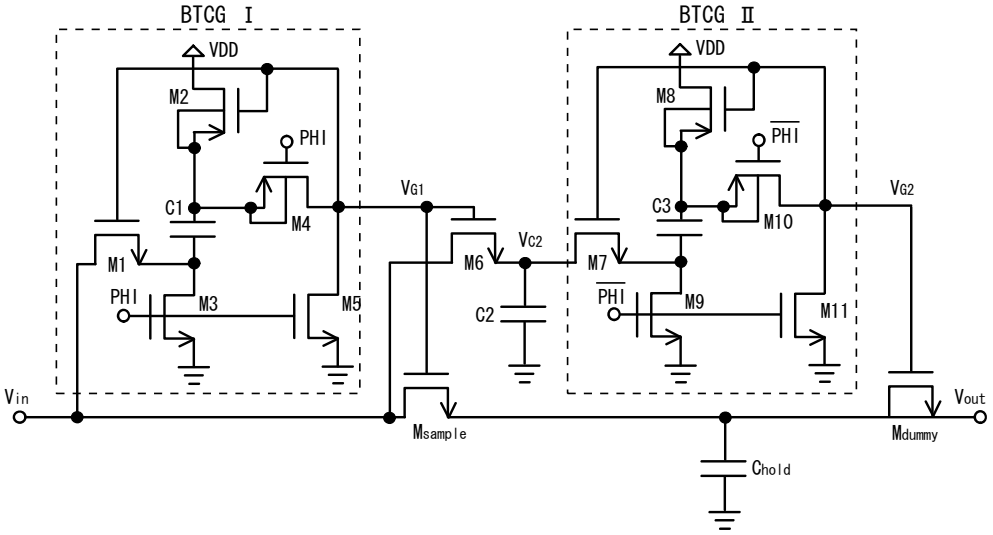

Figure 3: The proposed S/H circuit.

the ground level. When PHI is low, $M2$ and $M3$ are turned off, and $M1$ is turned on. The voltage of the top plate of $C1$ is boosted to $VDD + V_{in}$ because the bottom plate of $C1$ is connected to V_{in} and $M4$ and $M5$ are turned on and off, respectively. V_G, which is equal to the voltage of the top plate of $C1$, results in becoming $VDD + V_{in}$. In this way, the circuit shown in Fig. 1 generates the boosted and V_{in}-tracked clock.

Next, we discuss the error of the charge injection and the clock feedthrough. These effects cause the hold error of the S/H circuit. Especially, the hold error caused by these effects is increased when the boosted clock is used. In this paper, these problems are solved with a dummy switch (see Fig. 2), which is well-known technique.

If the channel electric charge flows into the drain and the source by halves, the electric charge (Δq_1) of M_{sample} is as follows [5].

$$\Delta q_1 = \frac{W_1 L_1 C_{ox}}{2}(V_{CK} - V_{in} - V_{TH}) \tag{1}$$

where W_1 and L_1 are the channel width and channel length of M_{sample}, respectively, C_{ox} is the gate oxide capacitance per unit area, V_{CK} is the amplitude of the clock PHI, V_{in} is the input signal, and V_{TH} is the threshold voltage of MOSFETs. Now, we define that W_2 and L_2 are the channel width and the channel length of the dummy switch (M_{dummy}), respectively. The electric charge (Δq_2) of M_{dummy} is as follows.

$$\Delta q_2 = W_2 L_2 C_{ox}(V_{CK} - V_{in} - V_{TH}) \tag{2}$$

Consequently, the influence of the charge injection can be reduced by setting to $W_2 = 0.5W_1$, $L_2 = L_1$ and $\overline{PHI} = \overline{V_{CK}}$.

The error voltage (ΔV) by clock feedthrough is given by [5]

$$\Delta V = V_{CK}\frac{WC_{ov}}{WC_{ov} + C_{hold}} \tag{3}$$

where C_{ov} is the gate-to-drain or the gate-to-source overlap capacitance. This causes the hold error in general. While, using the dummy switch, the error voltages by clock feedthrough of M_{sample} and M_{dummy} are given by [5]

$$\Delta V_{sample} = -V_{CK}\frac{W_1 C_{ov}}{W_1 C_{ov} + C_{hold} + 2W_2 C_{ov}} \tag{4}$$

$$\Delta V_{dummy} = V_{CK}\frac{2W_2 C_{ov}}{W_1 C_{ov} + C_{hold} + 2W_2 C_{ov}} \tag{5}$$

where ΔV_{sample} and ΔV_{dummy} are the error voltages caused by clock feedthrough of M_{sample} and M_{dummy}, respectively. Now we set $W_2 = 0.5W_1$ as mentioned above, $\Delta V_{sample} + \Delta V_{dummy}$ equals 0. That is to say, the error caused by the clock feedthrough can be completely cancelled.

Fig. 3 shows the proposed S/H circuit using the clock generators shown in Fig. 1 (BTCG I and II) and the dummy switch shown in Fig. 2. This circuit is controlled by the non-overlapped two phase clock (PHI and $\overline{PHI}$). In the proposed circuit, the BTCG I generates the feasible clock for the dummy switch in order to reduce the error caused by the charge injection and the clock feedthrough.

When PHI is low, $M6$ is turned on, and V_{in} is applied across $C2$. Simultaneously, V_{G2} becomes the ground level, therefore M_{dummy} is turned off. When PHI is high, $M6$ is turned off. The V_{C2} becomes equal to voltage just before $M6$ is turned off. And this voltage is inputted into the BTCG II. Therefore, the error caused by the charge injection and the clock feedthrough can be cancelled. In this way, we can archive the low-voltage, low-distortion and rail-to-rail S/H circuit.

3. Simulation Results

The proposed circuit has been evaluated through StarHSPICE simulation with the device parameters of 0.35μm

Table 1: Design parameters of the proposed circuit.

Device Name	Value
W/L of $M3$, $M6$, $M7$, $M9$, $M11$	5μm/0.5μm
W/L of $M2$, $M8$,	10μm/0.5μm
W/L of $M1$, $M4$, $M5$, $M10$	15μm/0.5μm
C_{hold}, $C2$	1.0pF
$C1$	1.5pF
$C3$	3.0pF

standard CMOS process. In the proposed circuit, a single supply voltage (VDD) of 1.5V is used. The other detailed settings are shown in Table 1.

Figs. 4a, 4b and 4c show the simulation results of the conventional circuit, the proposed circuit without the dummy switch and the proposed circuit with the dummy switch (Fig. 3) , respectively under the condition of the rail-to-rail input signal. From these figures, we can find that the proposed S/H circuit can operate well. Furthermore, we can find that the proposed S/H circuit with the dummy switch holds the V_{in} correctly with reducing the hold error.

Fig. 5 shows the relation between THD and amplitude of V_{in}. When the amplitude and the frequency of V_{in} are 1.5V$_{p-p}$ and 2.5MHz, respectively, THD of the proposed S/H circuit is 0.19%. Fig. 6 shows the relation between the hold error and amplitude of V_{in}. When the amplitude and the frequency of V_{in} are 1.0V$_{p-p}$ and 2.5MHz, respectively, we can find that the hold error is 1.8mV. Using the proposed S/H circuit with the dummy switch, we can see that the hold error can be reduced to 1/10 from Fig. 6.

4. Conclusions

In this paper, we have proposed a S/H circuit with the clock boost technique and the input signal tracking technique. The proposed circuit generates the clock with the amplitude of $VDD + v_{in}$, and the clock is used to control the MOS switch. By applying this circuit to a S/H circuit, we can deal with the rail-to-rail signal with maintainng low distortion. Furthermore, the hold error caused by the charge injection and the clock feedthrough can be also reduced by using the dummy switch. From the Star-HSPICE simulation, we have found that the hold error could be reduced to 1/10.

Acknowledgments

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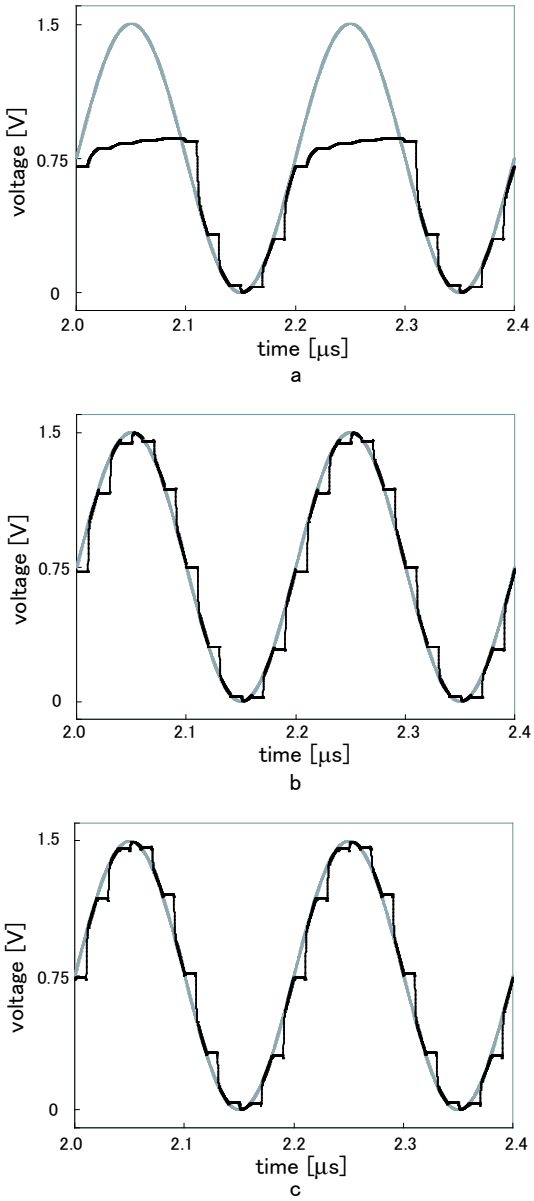

Figure 4: Simulation results. (a) Conventional (classical) S/H circuit, (b) the proposed S/H circuit without the dummy switch and (c) the proposed S/H circuit with the dummy switch (Fig. 3).

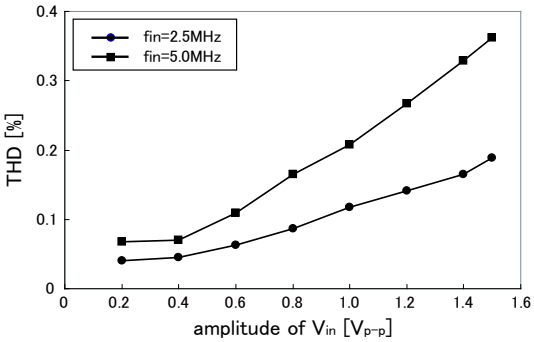

Figure 5: Simulated THD.

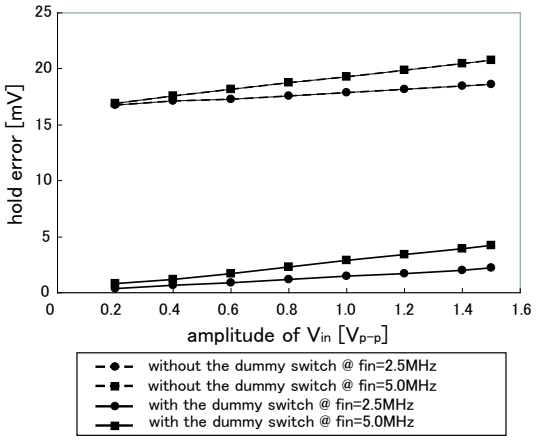

Figure 6: Simulated hold error.

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