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The Generalized DC Analysis of PWL Circuits by means of Polyhedral Circuits

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Abstract—The generalized DC analysis of generic piecewise-linear circuits includes some important problems of large interest as: search for all DC solutions, DC characterization of N-ports and search for DC working regions of circuits with tolerances in devices. A set-theoretical approach, based on the so-called polyhedral circuits, allows one to solve these problems in a unified way, leading to the formulation of a robust and efficient algorithm.

1. Introduction

In this paper, we focuse our attention on the generalized DC analysis of circuits whose nonlinear characteristics can be approximated by a piecewise-linear (PWL) implicit or explicit function [1].

A first important and popular problem consists of finding all the DC solutions of a resistive PWL circuit obtained by open circuiting the capacitors and short circuiting the inductors. A second important problem is the analysis of the characteristics of resistive PWL N-ports. Finding these characteristics for a generic circuits is, in general, very difficult. Note that the resultant characteristic of a one-port may consist of several separate branches, even if all embedded PWL elements have a one-branch characteristic. A third problem consists of finding the DC working regions of PWL circuits with tolerances in the devices characteristics, both linear and nonlinear. The solution of this problem is very important, because it is well known that semiconductor devices are subject to a large dispersion in their parameters, due to many reasons as aging, temperature effects and constructive techniques.

A theoretical instrument suitable to solve all the problems cited above, with a unified approach, is represented by the so-called polyhedral circuits, that are described by means of linear equalities and inequalities. Therefore, their solution domains are convex multidimensional polyhedra that can be found using Linear Programming (LP) techniques.

The aim of this paper is to show that this theoretical unified approach, already presented in [2], is not only robust and elegant, but it is also very powerful from a computational point of view.

2. The Theoretical Framework

Let us introduce the N-*augmented circuits*, obtained by connecting a norator to each port of a generic nonlinear N-port. From the view-point of classical circuit theory, any N-augmented circuit possesses infinitely many (in general ∞^N) solutions forming a set called *configuration domain*. Its projection onto the voltages and currents of the N ports coincides with the characteristic of the N-port. By convention, a 0-augmented circuit denotes any classical circuit without extra norators. Thus, the configuration domain of a 0-augmented circuit is constituted by its DC solutions. The considered N-augmented circuits contain M nonlinear elements, besides the norators. Their characteristics $f_m(x_m, y_m) = 0$, $m = 1, \ldots, M$, may be constituted either by a set of one-dimensional (1D) branches, or by a set of planar stripes, as it happens in the case of a circuit with tolerances. Indeed, a characteristic subject to dispersion of the parameters can be modelled with a stripe in the x_m-y_m plane, delimited by an upper and a lower characteristic set around the nominal one. A 1D characteristic can be approximated by a *1D PWL characteristic*, made up of the union of one or more chains of adjacent *1D segments* jointed in the *breakpoints* (Fig. 1a). A stripe characteristic can be approximated by a *spread PWL characteristic*, made up of the union of one or more chains of adjacent parallelograms, called hereafter *spread segments*, jointed in the *spread breakpoints* (Fig. 1b). In the sequel, the term *PWL characteristic* and the term *segment* will refer to both 1D and spread ones, since the next definitions and properties apply equally to both 1D and spread sets. The first and last segment (1D or spread) of each chain may be either bounded or unbounded. The number of segments defines the *rank* of the PWL characteristic.

A PWL characteristic can be partitioned into two or more portions, called *truncated PWL* (*T-PWL*) *characteristics*, each made up of one or more sequentially ordered segments (see Fig. 1). A set of T-PWL characteristics is said to be *complete* if each of the segments of the m-th original PWL characteristic belongs to one and only one T-PWL characteristic in the set.

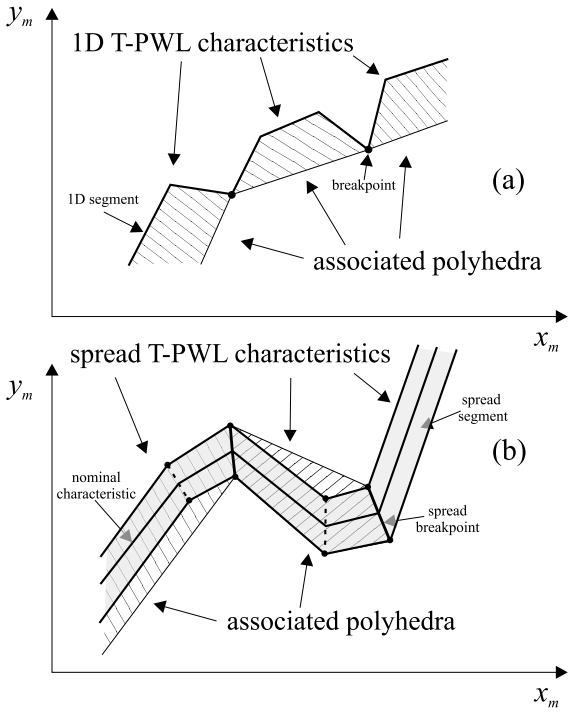

Figure 1: A complete set of T-PWL 1D and spread characteristics and the associated polyhedra.

When we substitute each PWL characteristic by one of its T-PWL characteristics, we obtain a *T-PWL N-augmented circuit*. The linear regions are suitable sets in which all T-PWL characteristics are reduced to segments (rank equal to 1). They can be separated in two classes: a linear region is said to be *admissible* if its configuration domain is not empty, otherwise, it is said to be *nonadmissible*. The product of the ranks of the M T-PWL characteristics is the rank of the T-PWL circuit and it corresponds to the number of linear regions contained in it. So, a set of T-PWL circuits is said complete if each linear region of the original PWL circuit belongs to one and only one T-PWL circuit in the set.

The hull of a generic set $\mathcal{A}$ is the most restricted convex set containing $\mathcal{A}$. For each T-PWL characteristic, we introduce the *associated polyhedron*, that is the associated hull (see Fig. 1). For a unit-rank T-PWL characteristic (a single segment), the hull coincides with the segment itself. We can now introduce the concept of *associated polyhedral N-augmented circuit*, as the circuit derived from a T-PWL N-augmented circuit by substituting each T-PWL characteristic with the associated polyhedron. For each polyhedral circuit, the configuration domain is a convex multidimensional polyhedron, exhibiting the following property.

Inclusion Property: The configuration domain of a T-PWL circuit, if not empty, is included into the configuration domain of the associated polyhedral circuit.

As a consequence, if the configuration domain of the associated polyhedral circuit is empty, then the configuration domain of the T-PWL circuit is, in turn, empty, while the contrary is not true. Analogously, if at least one linear region contained in the T-PWL circuit is admissible, also the associated polyhedral circuit is admissible. On the contrary, if all linear regions contained in a T-PWL circuit are nonadmissible, the associated polyhedral circuit may be either admissible or nonadmissible. This is due to the fact that the associated polyhedral circuit is the hull of the union of all embedded linear regions, and, therefore, may be more extended than the union itself. To test the configuration domain of an associated polyhedral circuit, we construct a Linear Programming (LP) problem, such that its feasible domain just coincides with the configuration domain, that is the solution domain, of the related associated polyhedral circuit. The emptyness of the configuration domain can be tested by means of Phase I, that is the procedure, well-known in LP, used for finding if the LP problem has a feasible domain.

The algorithm is structured according to a binary tree: each node of the tree represents simultaneously a specific T-PWL circuit, the associated polyhedral circuit and the two related configuration domains. The binary tree starts from the original PWL circuit, in which all PWL characteristics are complete and the related associated polyhedral circuit includes all linear regions. If its configuration domain is not empty, this node generates a complete set of two (first-generation nodes) T-PWL circuits, each one obtained by partitioning one of the M PWL characteristics into two T-PWL characteristics. We examine their corresponding configuration domains and, if they are not empty, they generate, in turn, four second-generation T-PWL circuits with the same rule, and so on. In principle, at each generation the number of T-PWL circuits increases exponentially by a factor of 2. Indeed, when the emptyness of the configuration domain proves that an associated polyhedral circuit is nonadmissible, the related T-PWL circuit, including all its linear regions, is deleted because it is nonadmissible too. For increasing order of generation the rank of the surviving T-PWL circuits decreases until linear regions are reached. If the configuration domain of a linear region is not empty, we can establish that it is admissible. The union of the admissible linear configuration domains coincides with the configuration domain of the original N-augmented PWL circuit.

3. DC Solution Problem

The DC solution problem consists in finding all the DC solutions of a PWL circuit. It is very important in the analysis of electrical circuits, also for determining their dynamical behaviour. All elements have 1D one-

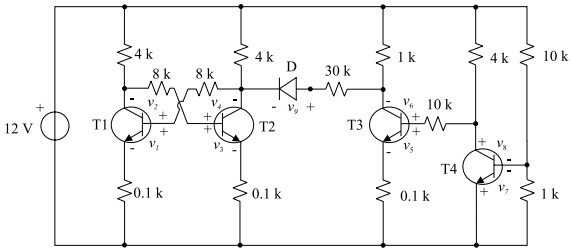

Figure 2: Circuit of DC solution problem.

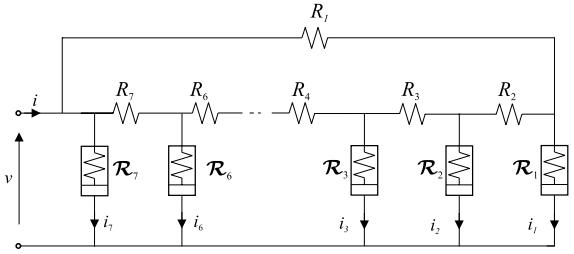

Figure 3: One-port example.

branch or multi-branch characteristics in $\mathcal{R}^2$, apart from possible couples nullators-norators: the solution domain is so formed, if the circuit is non pathological, by isolated points. The polyhedral circuits associated to the T-PWL circuits are generated adopting the method presented in [3]. Let us present one example, shown in Fig. 2. The algorithm has been implemented in C++ language on a PC with CPU 1400 MHz. The circuit contains 4 transistors and 1 exponential diode. The transitors are all modelled with the same Ebers-Moll model, with two exponential diodes and two current-controlled sources with parameters $\alpha_I = 0.2$ and $\alpha_F = 0.98$. The exponential diode has characteristic: $i = 10^{-9}(e^{-40v} - 1)$: it has been approximated at maximum with 80 segments. The maximum rank of the circuit is so $80^9 = 1.34\,10^{17}$, an impressive number. The circuit presents 3 solutions, listed in Ref. [4], while some data about the algorithm are shown in Table 1. Note that the algorithm is very efficient with each diode rank. Indeed, the number of solved polyhedral circuits is much smaller than the number of associated linear regions (rank) and the CPU time is reasonably small. Moreover, the precision obtained in the PWL approximations (80 segments) of the diode exponential characteristics provides a good accuracy in the solution values. If necessary, these can be initial conditions for traditional algorithms as Newton-Raphson, for example.

diodes rank	polyhedral circuits	CPU time [s]
20	369	1.1
32	435	1.9
80	483	3.7

Table 1: DC solution algorithm

4. N-Port Characteristic Problem

The characteristic of a generic one-port consists in the union of 1D segments, one for each admissible linear region, in the v-i plane [5]. When $N = 2$, the two-port may be represented by a pair of families of characteristics. A single characteristic of a family, for instance: $f_1(v_1, v_2, i_3 = i_3^0) = 0 \quad f_2(v_1 = v_1^0, i_3, i_4) = 0$, is obtained when one of the previous quantity, which

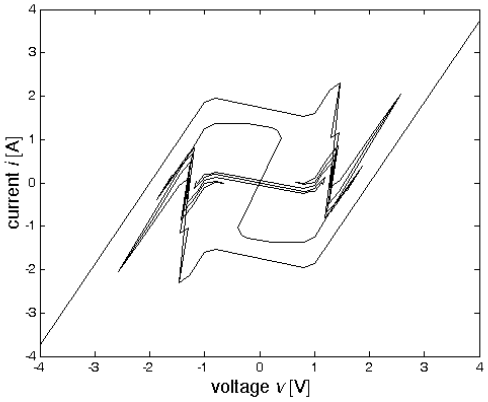

Figure 4: Characteristic of one-port in Fig. 3.

plays the role of family parameter, is fixed [6]. in general, for any N, the characteristic may be a N-dimensional manifold obtained examining the union of the configuration domains of the admissible linear regions. In this paper, we will show the results about the PWL one-port shown in Fig. 3. It is a nonlinear ring (see Ref. [7]) formed by 7 PWL resistive elements connected by 7 linear resistors of value 1.6 Ω. The PWL characteristic is formed by 5 segments: 3 finite segments with breakpoints $(-1, 1)$, $(-0.8, 0.9)$, $(0.8, -0.9)$ and $(1, -1)$ and two infinite segments with slope 1. The rank of the circuit is 78125. The characteristic, drawn in plane v-i (see Fig. 4), is formed by 195 segments. The algorithm needs to solve 15829 polyhedral circuits in about 5 s. Note that the characteristic presents some singular points and it is formed by many overlapping branches with many sharp turning points, therefore it presents some difficulties for other algorithms presented in literature.

5. DC Tolerance Analysis Problem

One of the greatest problems in electronics circuits consists in tolerances in elements characteristics, due to the dispersions of the related parameters [8]. As an example, the circuit shown in Fig. 5 is examined. The same Ebers-Moll model with two diodes and two current-controlled current sources has been

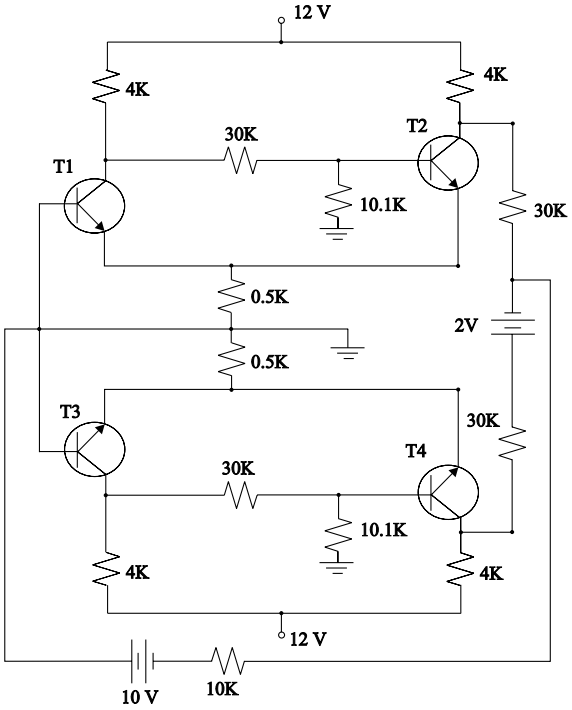

Figure 5: Circuit of tolerance analysis problem.

adopted for all transistors. Each exponential nominal characteristic of diodes has been approximated with 10 segments and the rank of the PWL circuit is 10^8. This circuit, with nominal characteristics for all diodes, has nine exact DC solutions [3]. We suppose that all four transistors, T1, T2, T3, and T4 have tolerances in their parameters. The PWL spread characteristic of each diode with tolerances has a width of about 20% in current respect the nominal value of the characteristic. This circuit presents 16 admissible linear regions, whose configuration domains are convex sets. The DC working regions are so formed by clusters of these configuration domains, as follows: 4 convex certain working regions, each one formed by the configuration domain of one linear region, and 5 non-convex certain working regions, each one formed by clusters of two or more linear regions, for a total of 9 certain working regions, corresponding to the DC solution points found with the nominal characteristics. The DC working regions are said to be *certain*, because a DC solution point certainly exists in the region for any choice of real characteristics inside the corresponding spread characteristics. The algorithm has analysed totally 815 polyhedral circuits in about 4.67 s, against the 541 polyhedral circuits and the 1.04 s of the nominal circuit. We see that the results obtained using the tolerance analysis are really good compared with the amount of simulations needed with the traditional algorithms.

6. Conclusions

The DC solution problem, the N-port characteristic problem and the DC tolerance analysis have been solved by introducing the polyhedral circuits. We investigated the effects of this unified approach, showing, by means of some examples, the power and efficiency of the derived algorithm. From a mathematical point of view, the algorithm adopting the polyhedral circuits is based on Linear Programming (LP) techniques, applied following the development of a binary tree. The next step will be to improve the precision and the efficiency of the algorithm, especially for large circuits.

References

[1] J. Vandewalle and L. Vanderberghe, "Piecewise-Linear Circuits and Piecewise-Linear Analysis," The Circuits and Filters Handbook, Editor Wai-Kai Chen, CRC Press, 1995.

[2] S. Pastore and A. Premoli, "DC Analysis of PWL Electric Networks and Sub-Networks by means of Set Theory", ISCAS 2003, Bangkok, Thailand, May 25-28, 2003, Vol. 3, pp. 658-661.

[3] S. Pastore and A. Premoli, "Polyhedral Elements: A New Algorithm for Capturing All the Equilibrium Points of Piecewise-Linear Circuits," IEEE Trans. Circuits Syst. I, vol. 40, no. 2, pp. 124–132, Feb. 1993.

[4] M. Tadeusiewicz and K. Glowienka, "A Contraction Algorithm for Finding All the DC solutions of Piecewise-Linear Circuits," Journal of Circuits, Systems, and Computers, vol. 4, no. 3, pp. 319–336, 1994.

[5] S. Pastore and A. Premoli, "Capturing All Branches of Any One-Port Characteristic in Piecewise-Linear Resistive Circuits," IEEE Trans. Circuits Syst., Part I, vol. CAS-43, no. 1, pp. 26–33, Jan. 1996.

[6] S. Pastore and A. Premoli, "Tracing any family of characteristics of a two-port composed of PWL resistive elements," NOLTA '93, Hawaii, USA, December 5-9, 1993, vol. 3, pp. 847–852.

[7] S. Pastore, "Detection of All the Equilibrium Points of Dynamic 1D Autonomous Ring", 14th ECCTD, Stresa, Italy, Aug.29-Sept. 2, 1999, Part II, pp. 699-702.

[8] S. Pastore and A. Premoli, "DC Tolerance of Electronic Circuits by Linear Programming Techniques", ISCAS 2001, Sydney, Australia, May 6-9, 2001 , Vol. 3, pp. 369-372.