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A DC-AC Inverter Using Switched-Capacitor Techniques

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Abstract—In this paper, a DC-AC inverter using a switched-capacitor (SC) technique is proposed. Since the proposed SC DC-AC inverter includes no magnetic elements, it can provide us small volume and light weight. The inverter is designed by adding a polarity exchange circuit and $N + 1$ ($N = 2, 3, \ldots$) power-switches to a Dickson-type DC-DC converter.Therefore, the proposed circuit can generate not only a DC-DC output but a DC-AC output. By exploiting a pulse amplitude modulation (PAM) method, the inverter can generate various types of AC outputs. Furthermore, to alleviate the distortion, the output voltage is regulated by controlling the on-resistances of the power-switches. The validity of the circuit design is confirmed through SPICE simulations. The SPICE simulations show the following results: 1. the efficiency of DC-AC inverter is more than 86 % when the input voltage $V_{in} = 24V$ and the output load 200Ω and 2. various types of AC outputs can be generated.

1. Introduction

In electronic products, power transformers are indispensable, and the power transformers using magnetic elements are used widely. Although the power transformers employing magnetic elements are very efficient, the demands of small volume and light weight has been increasing in the design of the power transformers. The cause of the increase of volume and weight is the existence of magnetic elements. To satisfy such requirements, we focused on switched-capacitor (SC) techniques. The power transformers which are designed by using SC techniques can realize small-volume and light-weight since they require no magnetic elements. Until now, several types of power transformers have been designed by using SC techniques [1]-[8]. The waveform of the output voltage is determined by the number of capacitors since SC power transformers convert the values of DC voltages by changing the connection of capacitors. Hence, in the design of DC-AC inverters using SC techniques, the distortion of the output voltage is occurred [5]-[8].

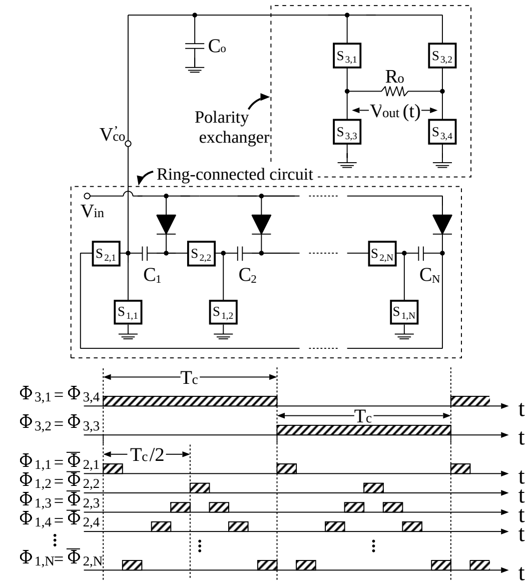


Fig.1 Conventional DC-AC inverter proposed in [5]. (Conventional inverter-1)

In this paper, a DC-AC inverter using an SC technique is proposed. Since the proposed SC DC-AC inverter includes no magnetic elements, it can provide us small volume and light weight. The inverter is designed by adding a polarity exchange circuit and $N + 1$ ($N = 2, 3, \ldots$) power-switches to a Dickson-type DC-DC converter. Therefore, the proposed circuit can generate not only a DC-DC output but a DC-AC output. By exploiting a pulse amplitude modulation (PAM) method, the circuit can generate various types of AC outputs. Furthermore, to alleviate the distortion, the output voltage is regulated by controlling the on-resistances of the power-switches. Concerning a 6-stage DC-AC inverter, SPICE simulations are performed to confirm the validity of the circuit design.

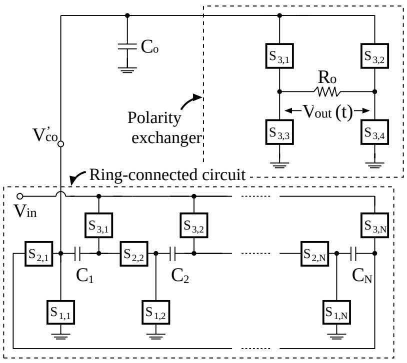


Fig.2 Modified conventional DC-AC inverter. (Conventional inverter-2)

2. Circuit Structure

2.1. Conventional DC-AC Inverter

Figure 1 shows the conventional SC DC-AC inverter [1] proposed by Hara et al. [5]. In the conventional inverter-1 of Fig.1, the triangular voltage is generated from the ring-connected circuit which consists of $2N$ switches, N diodes, and $N+1$ capacitors. In Fig.1, the switch $S_{1,j}$ $(j = 1, 2, \ldots, N)$ is driven by non-overlapped N-phase pulses $\Phi_{1,j}$, and the clock pulse $\Phi_{2,j}$ for $S_{2,j}$ is set to the inverted pulses of $\Phi_{1,j}$. When $C_o = 0$ [2] and the voltage-drop caused by switching-elements is free, the output of Fig.1 is given by

$$V_{co}^{'} = (Q(t) - 1)\ V_{in}, \qquad (1)$$

where $Q(t)$ $(\in \{1, 2, \ldots, N\})$ denotes the number of the capacitors connected to the output terminal. In the polarity exchanger, the voltage $V_{co}^{'}$ is reversed its polarity every one period T_c which starts from $0V$. However, the threshold voltage drop of these diodes affects the efficiency of the inverter. The effect of the threshold voltage drop can be avoided by replacing the diodes with the switches.

Figure 2 shows the modified DC-AC inverter. The conventional circuit-2 consists of $3N$ switches and $N+1$ capacitors. In the case of Fig.2, the output is given by

$$V_{co}^{'} = \frac{(Q(t) - 1)}{P(t)}\ V_{in}, \qquad (2)$$

where $P(t)$ $(\in \{1, 2, \ldots, N\})$ denotes the number of the capacitors connected to the input terminal. The voltage $V_{co}^{'}$ is also reversed its polarity every one period in the polarity exchanger.

As Eqs.(1) and (2) show, the number of stages of stairs-waveforms is determined by the numbers of capacitors C_j. The unevenness of $V_{co}^{'}$ can be smoothed out by using a mass capacitor C_o. However, it leads to the increase in hardware cost.

[1]In Fig.1, the circuits to provide clock pulses are omitted.

[2]The capacitor C_o is used to smooth out the unevenness of $V_{co}^{'}$.

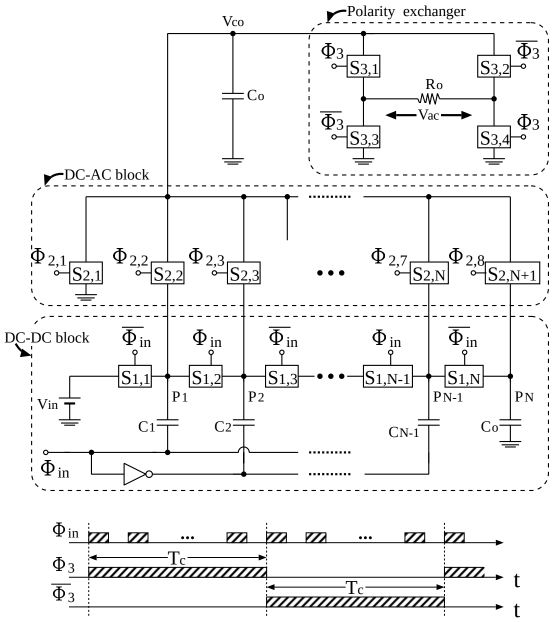


Fig.3 Proposed power inverter.

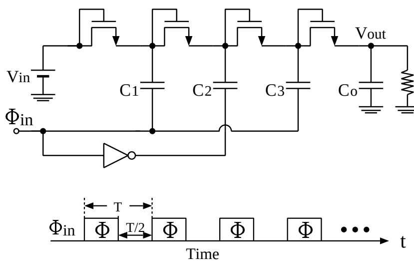


Fig.4 3-stage Dickson-type DC-DC converter.

2.2. Proposed Power Inverter

Figure 3 shows the proposed DC-AC inverter. The inverter is designed by adding a polarity exchange circuit and $N+1$ $(N = 2, 3, \ldots)$ power-switches to a Dickson-type DC-DC converter. The DC-DC block in Fig.3 is an N-stage Dickson-type DC-DC converter. The Dickson-type converter consists of N diodes and N capacitors. Figure 4 shows a 3-stage Dickson-type DC-DC converter which is designed by using NMOS-diodes [1]. In Fig.4, each capacitor is connected in series via diode-connected NMOSFET's. Therefore, a threshold voltage drop is occurred by NMOS-diodes. In the proposed DC-AC inverter, these diodes are replaced by the power switches $S_{1,j}$'s in order to avoid the voltage drop. In the DC-DC block, the voltages V_m $(m \in \{1, 3, 5, \ldots\})$ and V_n $(n \in \{2, 4, 6, \ldots\})$ of

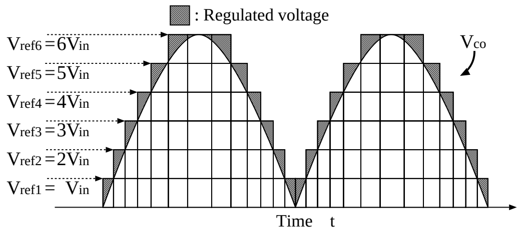


Fig.5 An example of the regulated AC outputs in case of a sine wave.

nodes P_j's are given by

$$V_m = \begin{cases} (m+1)V_{in} & \text{if} \quad \Phi_{\text{in}} = High, \\ mV_{in} & \text{if} \quad \Phi_{\text{in}} = Low, \end{cases} \quad (3)$$

$$V_n = \begin{cases} nV_{in} & \text{if} \quad \Phi_{\text{in}} = High, \\ (n+1)V_{in} & \text{if} \quad \Phi_{\text{in}} = Low, \end{cases} \quad (4)$$

where

$$V_N = NV_{in}.$$

The stepped-up DC voltage can be obtained from the node P_N.

In the DC-AC block of Fig.3, the DC-AC conversion is achieved by controlling non-overlapped clock pulses $\Phi_{2,j}$. The node voltages of Eqs.(3) and (4) are sampled via $S_{2,j}$'s. Hence the waveform of the AC output is determined by the timing of the clock pulses for $S_{2,j}$'s. When $C_o = 0$, the AC output is given by

$$V_{co} = \begin{cases} V_j & \text{if} \quad S_{2,1} = Off, \\ 0 & \text{if} \quad S_{2,1} = On. \end{cases} \quad (5)$$

As Eqs.(3) $\sim$ (5) show, the waveform of the AC output depends on the number of capacitors. To smooth out the unevenness of AC output, the AC output is regulated by controlling the on-resistances of the power-switches. An example of the regulated AC outputs is shown in Fig.5. The hatched area in Fig.5 is the regulated voltage by the on-resistances control. In the case of a sine wave, the voltage V_j is sampled as

$$V_{co} = V_{j+1} \quad \text{if} \quad t_j \le t < t_{j+1}, \quad (6)$$

where t_j and t_{j+1} satisfies

$$V_j = \sin(t_j) \quad \text{and} \quad V_{j+1} = \sin(t_{j+1}).$$

In the polarity exchanger, the voltage V_{co} is reversed its polarity every one period T_c which starts from $0V$.

3. Simulation

Figure 6 shows an example of the proposed DC-AC inverters when $N = 6$ [3]. To confirm the validity of circuit design, SPICE simulations were performed concerning the circuits shown in Figs.1, 2 and 6. The SPICE simulations were performed under the conditions that $V_{in} = 24V$ and $C_i = 300\mu F$.

[3] In the case of Fig.6, V_{co} satisfies $V_{co} \in \{0, V_{in}, 2V_{in}, 3V_{in}, 4V_{in}, 5V_{in}, 6V_{in}\}$ when $C_o = 0F$.

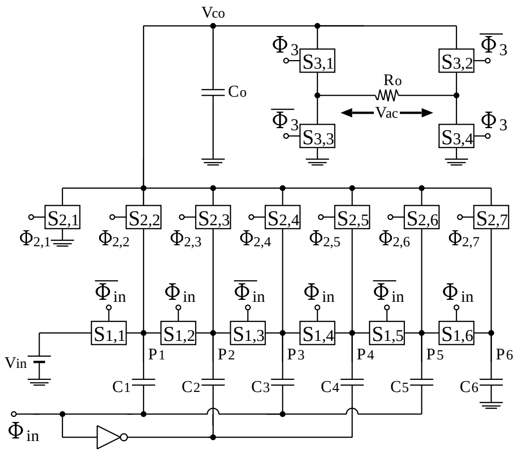


Fig.6 An example of the proposed DC-AC inverters when $N = 6$.

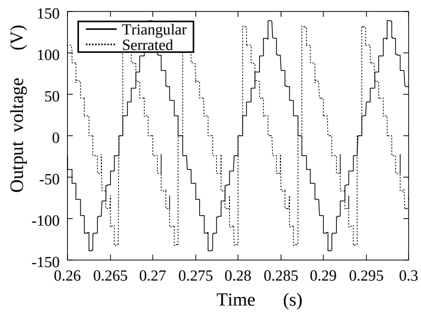
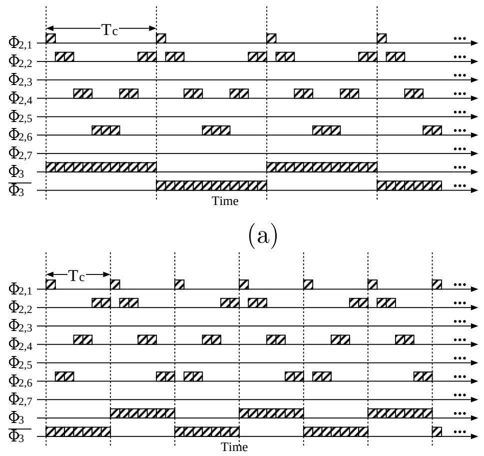


Fig.7 Simulated DC-AC outputs.

Figure 7 shows the DC-AC outputs generated by the proposed circuit of Fig.6. In the simulations, the clock pulses for $S_{i,j}$ were set to as shown in Fig.8, and the output capacitor C_o was set to $0F$. To compare with the conventional inverters, the waveforms of Fig.7 were not regulated. As Fig.7 shows, the proposed circuit can generate various types of AC outputs. Figure 9 shows the DC-AC outputs generated by the conventional inverter-1 and 2. In the simulations of Fig.9, the parameter N was set to 7. The loss of the DC-AC conversion of the conventional inverter-2 is smaller than that of the conventional circuit-1. As Figs.7 and 9 show, the output waveforms of the proposed circuit and the conventional circuit-2 are almost same. However, the material cost for the proposed circuit is smaller than that of the conventional circuit-2. Table 1 shows the material cost for these inverters. Figure 10 shows the regulated DC-AC output of the proposed circuit. The AC output of Fig.10 was regulated by controlling the on-resistances of $S_{2,j}$. In Fig.10, the



(a)

(b)

Fig.8 Timing of the clock pulses in the case of DC-AC conversion. (a) Triangular waveform. (b) Serrated waveform.

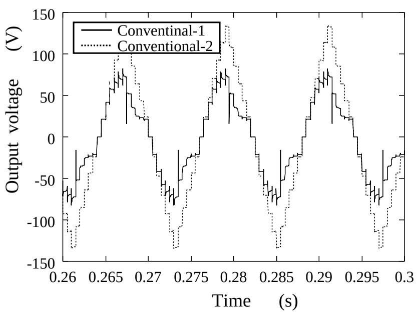


Fig.9 Simulated DC-AC outputs of the conventional inverters.

output load R_o was set to 200Ω. The efficiency of the proposed inverter is more than 86 %.

4. Conclusion

A DC-AC inverter using an SC technique has been proposed in this paper.

The SPICE simulations show the following results: 1. the efficiency of DC-AC conversion is more than 86 % when the input voltage $V_{in} = 24V$, 2. various types of AC outputs can be generated and 3. the proposed circuit can reduce the hardware cost.

The further improvement of efficiency is left to the future study.

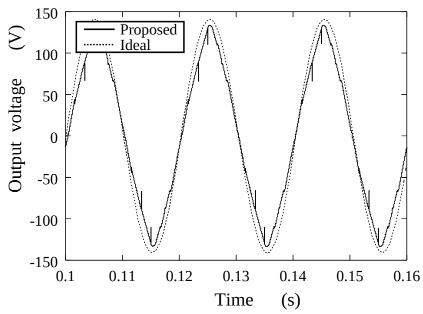


Fig.10 Simulated DC-AC outputs when $R_o = 200\Omega$.

Table 1 Material cost.

	Power switch	Diode	Capacitor
Proposed circuit	19	0	8
Conventional circuit-1	20	8	9
Conventional circuit-2	28	0	9

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